

TPS20xxB-Q1 Current-Limited Power-Distribution Switches

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: -40°C to 125°C ambient operating temperature range
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C6
 - Device MM ESD classification level M0
- 105-m Ω high-side MOSFET
- 500-mA continuous current
- Thermal and short-circuit protection
- Accurate current limit: 0.75 A (minimum), 1.25 A (maximum)
- Operating range: 2.7 V to 5.5 V
- 0.6-ms typical rise time
- Undervoltage lockout
- Deglitched fault report ($\overline{\text{OC}}$)
- No $\overline{\text{OC}}$ glitch during power up
- Maximum standby supply current: 1 μA (single, dual) or 2 μA (triple, quad)
- Bidirectional switch
- UL recognized under file number E169910

2 Applications

- Heavy Capacitive Loads
- Short-Circuit Protection

3 Description

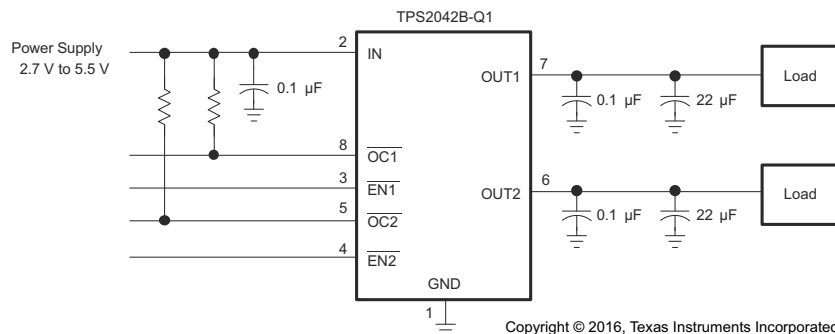
The TPS20xxB-Q1 power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporate 105-m Ω N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{\text{OCx}}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1 A (typical).

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2041B-Q1	SOT-23 (5)	2.80 mm \times 2.90 mm
TPS2042B-Q1, TPS2051B-Q1	SOIC (8)	4.90 mm \times 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic



Table of Contents

1 Features	1	9 Application and Implementation	13
2 Applications	1	9.1 Application Information.....	13
3 Description	1	9.2 Typical Applications.....	13
4 Revision History	2	10 Power Supply Recommendations	20
5 Pin Configuration and Functions	3	11 Layout	21
6 Specifications	4	11.1 Layout Guidelines.....	21
6.1 Absolute Maximum Ratings.....	4	11.2 Layout Example.....	21
6.2 ESD Ratings.....	4	11.3 Thermal Considerations.....	21
6.3 Recommended Operating Conditions.....	5	12 Device and Documentation Support	22
6.4 Thermal Information.....	5	12.1 Related Links.....	22
6.5 Electrical Characteristics.....	5	12.2 Receiving Notification of Documentation Updates.....	22
6.6 Typical Characteristics.....	7	12.3 Support Resources.....	22
7 Parameter Measurement Information	9	12.4 Trademarks.....	22
8 Detailed Description	10	12.5 Electrostatic Discharge Caution.....	22
8.1 Overview.....	10	12.6 Glossary.....	22
8.2 Functional Block Diagrams.....	10	13 Mechanical, Packaging, and Orderable Information	22
8.3 Feature Description.....	11		
8.4 Device Functional Modes.....	12		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2016) to Revision D (October 2020)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document.....	1
• Changed "70-mΩ High-Side MOSFET" to "105-mΩ High-Side MOSFET" in the <i>Features</i> list.....	1
• Changed "70-mΩ High-Side MOSFET" to "105-mΩ High-Side MOSFET" in the <i>Description</i> section.....	1
• Updated $r_{DS(ON)}$ TYP and MAX values in the <i>Electrical Characteristics</i> table.....	5
• Updated Figure 6-9	7
• Changed "70-mΩ High-Side MOSFET" to "105-mΩ High-Side MOSFET" in the <i>Overview</i> section.....	10
Changes from Revision B (October 2011) to Revision C (September 2016)	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet.....	1
• Deleted General Switch Catalog image.....	1
• Added AEC-Q100 Qualified bullets.....	1
• Added <i>Thermal Information</i> table.....	5
• Deleted <i>Dissipation Ratings</i> section	7
• Combined Functional Block Diagrams for TPS2041B-Q1 and TPS2051B-Q1 as they are the same.....	10
Changes from Revision A (June 2010) to Revision B (October 2011)	Page
• Changed orderable part number From: TPS2041QDBVRQ1 To: TPS2041BQDBVRQ1.....	1
Changes from Revision * (November 2007) to Revision A (June 2010)	Page
• Added the TPS2041B-Q1 device information.....	1

5 Pin Configuration and Functions

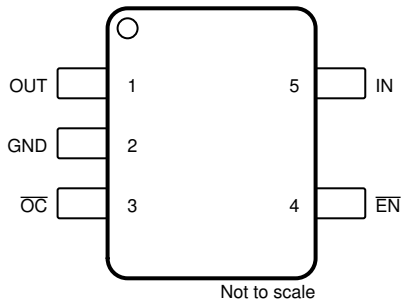


Figure 5-1. TPS2041B-Q1 DBV Package 5-Pin SOT-23 Top View

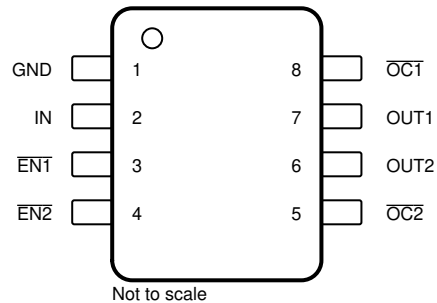


Figure 5-2. TPS2042B-Q1 D Package 8-Pin SOIC Top View

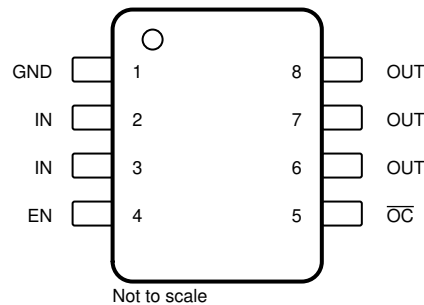


Figure 5-3. TPS2051B-Q1 D Package 8-Pin SOIC Top View

Table 5-1. Pin Functions: TPS2041B-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	4	I	Enable input, logic low turns on power switch
GND	2	GND	Ground
IN	5	PWR	Supply input voltage
OC	3	O	Overcurrent, open-drain output, active low
OUT	1	O	Power-switch output

Table 5-2. Pin Functions: TPS2042B-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN1	3	I	Enable input, logic low turns on power switch IN-OUT1
EN2	4	I	Enable input, logic low turns on power switch IN-OUT2
GND	1	GND	Ground
IN	2	PWR	Supply input voltage
OC1	8	O	Overcurrent, open-drain output, active low, IN-OUT1
OC2	5	O	Overcurrent, open-drain output, active low, IN-OUT2

Table 5-2. Pin Functions: TPS2042B-Q1 (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
OUT1	7	O	Power-switch output, IN-OUT1
OUT2	6	O	Power-switch output, IN-OUT2

Table 5-3. Pin Functions: TPS2051B-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	4	I	Enable input, logic high turns on power switch
GND	1	GND	Ground
IN	2, 3	PWR	Supply input voltage
\overline{OC}	5	O	Overcurrent open-drain output, active low
OUT	6, 7, 8	O	Power-switch output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted⁽¹⁾

		MIN	MAX	UNIT
Input voltage ⁽²⁾	IN	-0.3	6	V
Output voltage ⁽²⁾	OUT, OUTx	-0.3	6	V
Input voltage	\overline{ENx} , EN	-0.3	6	V
Voltage, $V_{I(\overline{OC})}$, $V_{I(\overline{OCx})}$	\overline{OC} , \overline{OCx}	-0.3	6	V
Continuous output current		Internally limited		
Continuous total power dissipation		See ESD Ratings		
Operating virtual-junction temperature, T_J		-40	125	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND.

6.2 ESD Ratings

		VALUE	UNIT
TPS2041B-Q1 in DBV Package and TPS2042B-Q1 in D package			
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2500
		Charged-device model (CDM), per AEC Q100-011	±1500
		Machine model (MM), per AEC Q100-003	±50
TPS2051B-Q1 in D package			
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	±1500
		Machine model (MM), per AEC Q100-003	±50

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{I(IN)}$	Input voltage (IN)	2.7	5.5	V
$V_{I(EN\bar{x})}$, $V_{I(EN)}$	Input voltage (\bar{ENx} , EN)	0	5.5	V
$I_{O(OUT)}$, $I_{O(OUTx)}$	Continuous output current (OUT, OUTx)	0	500	mA
T_J	Operating virtual-junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS2041B-Q1	TPS2042B-Q1	TPS2051B-Q1	UNIT
		DBV (SOT-23)	D (SOIC)	D (SOIC)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.1	117.2	124.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	131.2	63.3	72.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.4	57.5	64.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.2	15.3	24.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.3	37	64.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating junction temperature range, $V_{I(IN)} = 5.5$ V, $I_O = 0.5$ A, $V_{I(EN\bar{x})} = 0$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(ON)}$	Static drain-source on-state resistance, 5-V or 3.3-V operation	$V_{I(IN)} = 5$ V or 3.3 V, $I_O = 0.5$ A	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		105	160	mΩ
	Static drain-source on-state resistance, 2.7-V operation ⁽²⁾	$V_{I(IN)} = 2.7$ V, $I_O = 0.5$ A	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		110	175	
t_r	Rise time, output ⁽²⁾	$V_{I(IN)} = 5.5$ V $V_{I(IN)} = 2.7$ V	$C_L = 1$ μF, $R_L = 10$ Ω $T_J = 25^\circ\text{C}$		0.6 0.4	1.5 1	ms
t_f	Fall time, output ⁽²⁾	$V_{I(IN)} = 5.5$ V $V_{I(IN)} = 2.7$ V	$C_L = 1$ μF, $R_L = 10$ Ω $T_J = 25^\circ\text{C}$		0.05 0.05	0.5 0.5	
ENABLE INPUT (EN, ENx)							
V_{IH}	High-level input voltage	2.7 V $\leq V_{I(IN)} \leq 5.5$ V		2			V
V_{IL}	Low-level input voltage	2.7 V $\leq V_{I(IN)} \leq 5.5$ V				0.8	
I_I	Input current	$V_{I(EN\bar{x})} = 0$ V or 5.5 V		-0.5		0.5	μA
t_{on}	Turnon time ⁽²⁾	$C_L = 100$ μF, $R_L = 10$ Ω				3	ms
t_{off}	Turnoff time ⁽²⁾	$C_L = 100$ μF, $R_L = 10$ Ω				10	
CURRENT LIMIT							
I_{OS}	Short-circuit output current	$V_{I(IN)} = 5$ V, OUT connected to GND, device enabled into short-circuit	$T_J = 25^\circ\text{C}$	0.65	1	1.25	A
			$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	0.6	1	1.3	
SUPPLY CURRENT (TPS2041B-Q1, TPS2051B-Q1)							
Supply current, low-level output	No load on OUT, $V_{I(EN)} = 5.5$ V or $V_{I(EN)} = 0$ V	$T_J = 25^\circ\text{C}$		0.5	1	μA	
		$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		0.5	5		
Supply current, high-level output	No load on OUT, $V_{I(EN)} = 0$ V or $V_{I(EN)} = 5.5$ V	$T_J = 25^\circ\text{C}$		43	60	μA	
		$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		43	70		
Leakage current	OUT connected to ground, $V_{I(EN)} = 5.5$ V or $V_{I(EN)} = 0$ V	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		1		μA	
Reverse leakage current	$V_{I(OUTx)} = 5.5$ V, IN = ground ⁽²⁾	$T_J = 25^\circ\text{C}$		0		μA	

6.5 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = 0.5\text{ A}$, $V_{I(\overline{ENx})} = 0\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (TPS2042B-Q1)					
Supply current, low-level output	No load on OUT, $V_{I(\overline{ENx})} = 5.5\text{ V}$	$T_J = 25^\circ\text{C}$	0.5	1	μA
		$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	0.5	5	
Supply current, high-level output	No load on OUT, $V_{I(\overline{ENx})} = 0\text{ V}$	$T_J = 25^\circ\text{C}$	50	70	μA
		$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$	50	90	
Leakage current	OUT connected to ground, $V_{I(\overline{ENx})} = 5.5\text{ V}$	$-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$		1	μA
Reverse leakage current	$V_{I(\text{OUTx})} = 5.5\text{ V}$, IN = ground ⁽²⁾	$T_J = 25^\circ\text{C}$		0.2	μA
UNDERVOLTAGE LOCKOUT					
Low-level input voltage, IN, INx		2		2.5	V
Hysteresis, IN, INx	$T_J = 25^\circ\text{C}$		75		mV
OVERCURRENT ($\overline{\text{OC}}$, $\overline{\text{OCx}}$)					
Output low voltage, $V_{OL(\overline{\text{OCx}})}$	$I_{O(\overline{\text{OCx}})} = 5\text{ mA}$			0.4	V
OFF-state current ⁽²⁾	$V_{O(\overline{\text{OCx}})} = 5\text{ V}$ or 3.3 V			1	μA
$\overline{\text{OC}}$ deglitch ⁽²⁾	$\overline{\text{OCx}}$ assertion or deassertion	4	8	15	ms
THERMAL SHUTDOWN⁽³⁾					
Thermal shutdown threshold ⁽²⁾		135			$^\circ\text{C}$
Recovery from thermal shutdown ⁽²⁾		125			$^\circ\text{C}$
Hysteresis ⁽²⁾			10		$^\circ\text{C}$

- (1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be accounted for separately.
- (2) Specified by design.
- (3) The thermal shutdown only reacts under overcurrent conditions.

6.6 Typical Characteristics

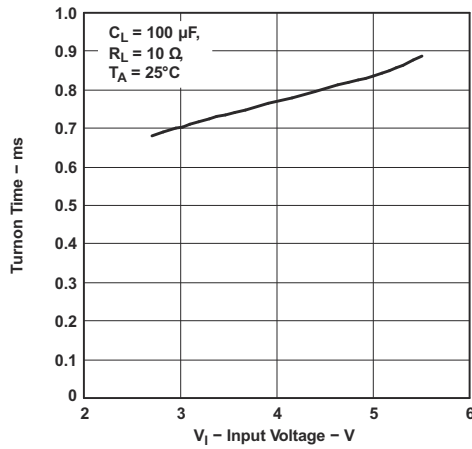


Figure 6-1. Turnon Time vs Input voltage

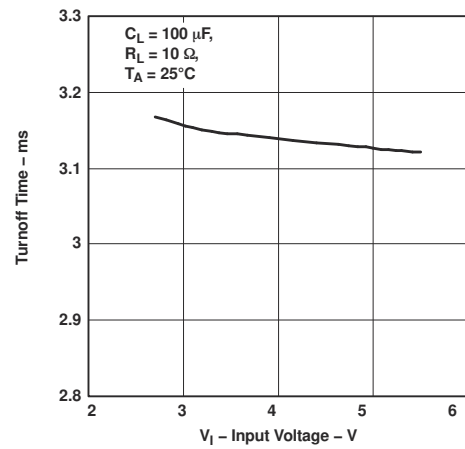


Figure 6-2. Turnoff Time vs Input Voltage

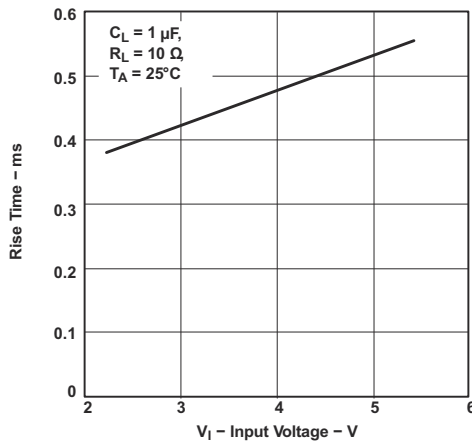


Figure 6-3. Rise Time vs Input Voltage

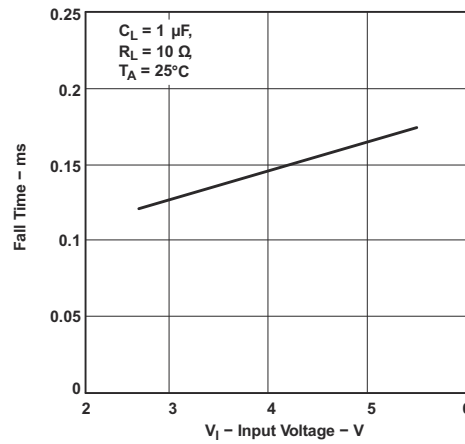


Figure 6-4. Fall Time vs Input Voltage

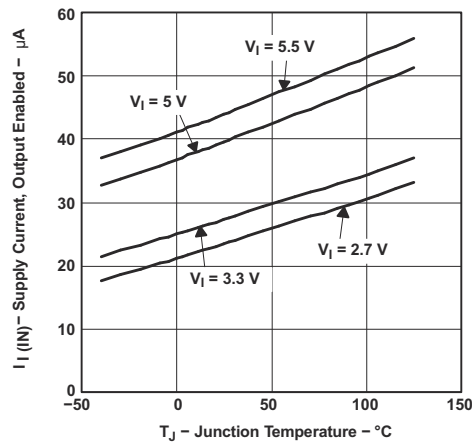


Figure 6-5. TPS2041B-Q1 and TPS2051B-Q1 Supply Current, Output Enabled vs Junction Temperature

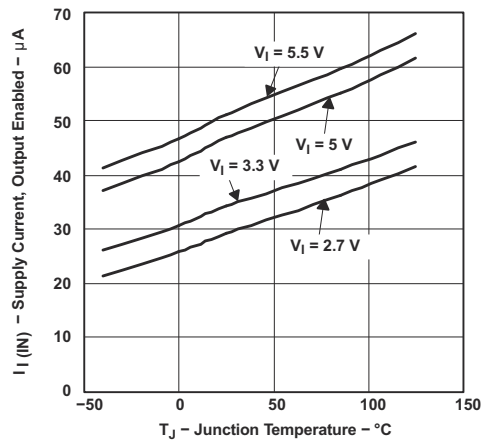


Figure 6-6. TPS2042B-Q1 Supply Current, Output Enabled vs Junction Temperature

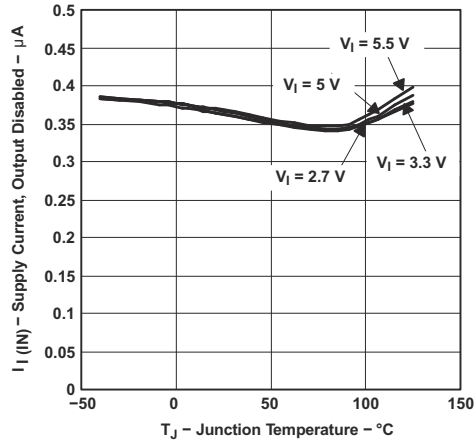


Figure 6-7. TPS2041B-Q1 and TPS2051B-Q1 Supply Current, Output Disabled vs Junction Temperature

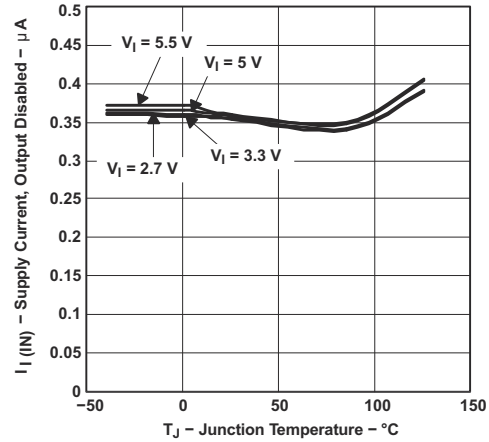


Figure 6-8. TPS2042B-Q1 Supply Current, Output Disabled vs Junction Temperature

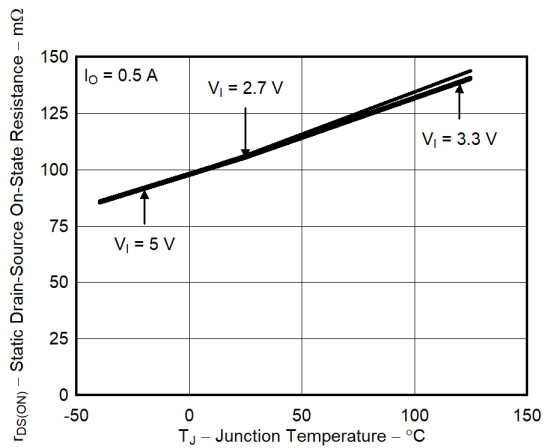


Figure 6-9. Static Drain-Source ON-state Resistance vs Junction Temperature

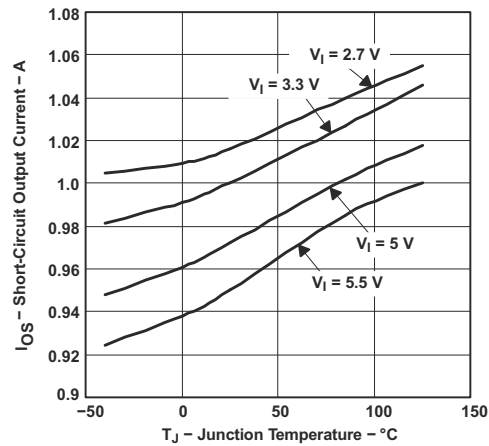


Figure 6-10. Short-Circuit Output Current vs Junction Temperature

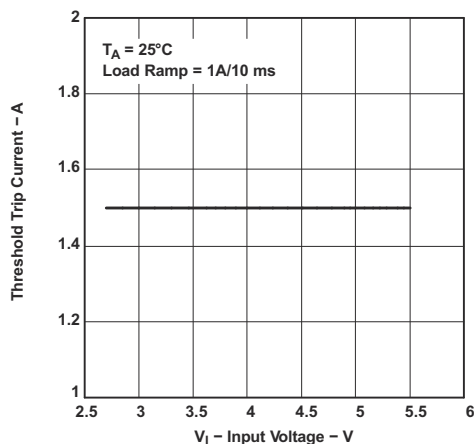


Figure 6-11. Threshold Trip Current vs Input Voltage

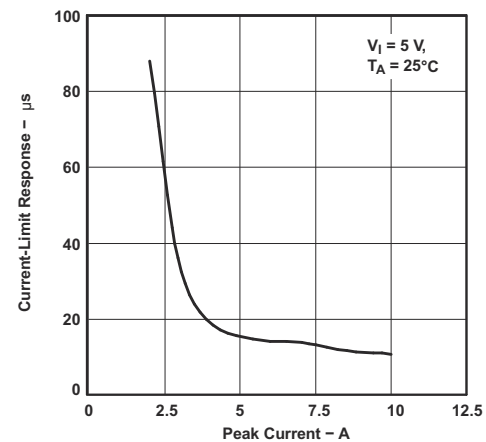


Figure 6-12. Current-Limit Response vs Peak Current

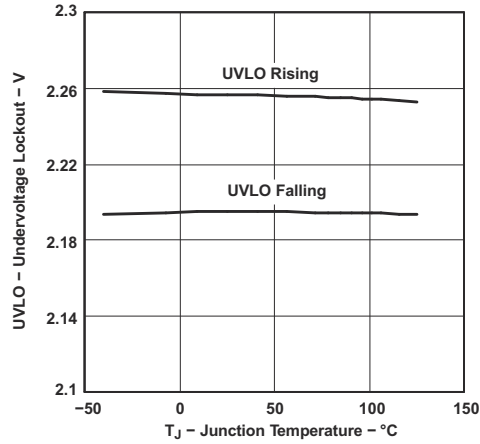


Figure 6-13. Undervoltage Lockout vs Junction Temperature

7 Parameter Measurement Information

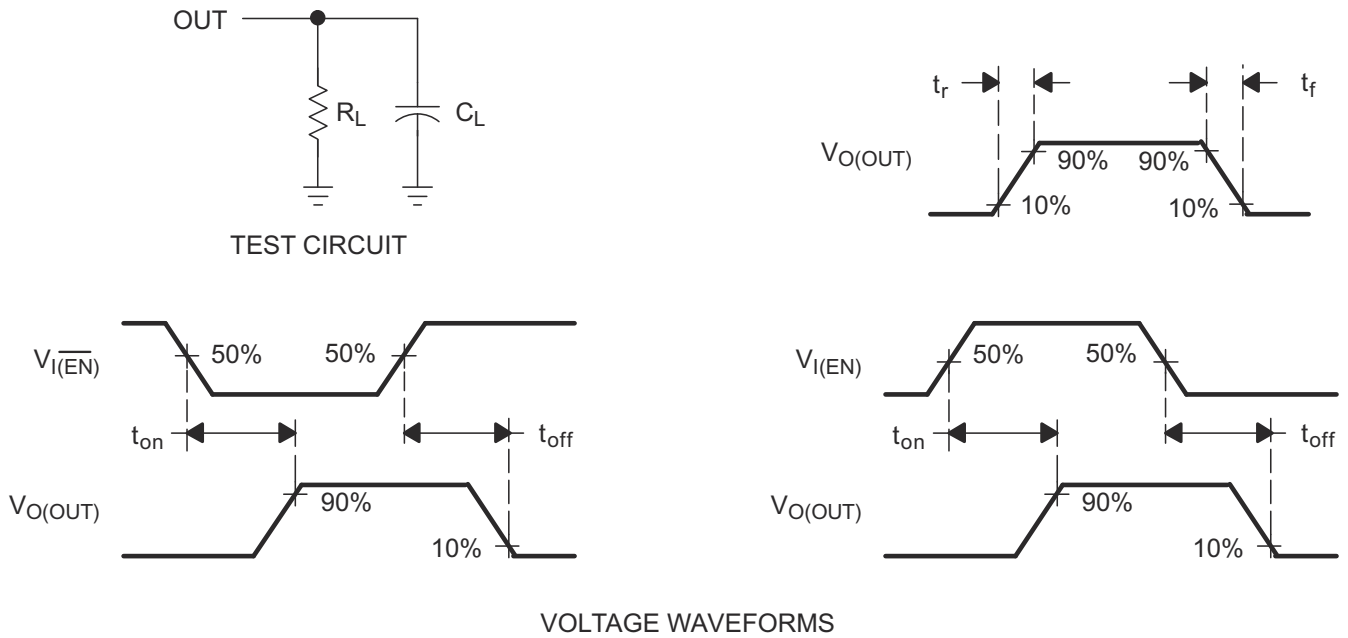


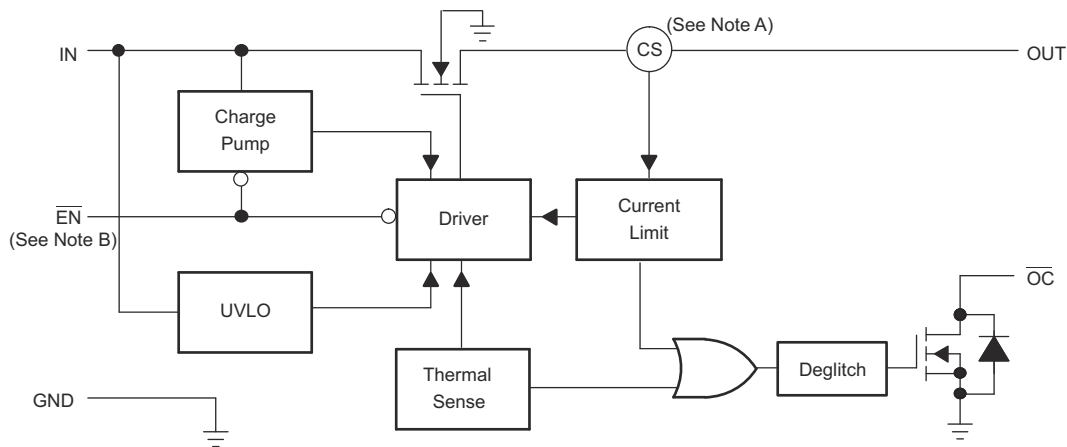
Figure 7-1. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TPS20xxB-Q1 devices are current-limited, power-distribution switches providing 0.5-A continuous-load current. These devices incorporate 105-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. A gate driver is provided by an internal charge pump designed to minimize current surges during switching. The charge pump requires no external components and allows operation supplies as low as 2.7 V.

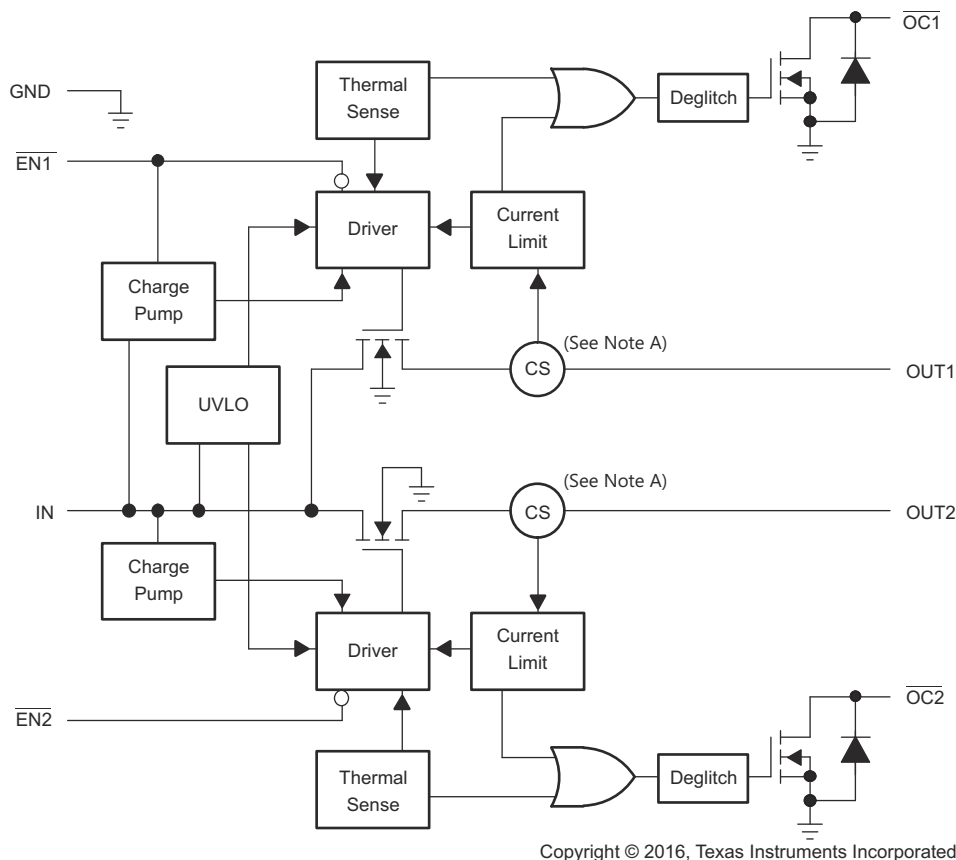
8.2 Functional Block Diagrams



Copyright © 2016, Texas Instruments Incorporated

- A. CS = Current sense
- B. EN = Active low ($\overline{\text{EN}}$) for TPS2041B-Q1; Active high (EN) for TPS2051B-Q1

Figure 8-1. Functional Block Diagram (TPS2041B-Q1 and TPS2051B-Q1)



A. CS = Current sense

Figure 8-2. Functional Block Diagram (TPS2042B-Q1)

8.3 Feature Description

8.3.1 Power Switch

The power switch is an N-channel MOSFET with a low ON-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 500 mA.

8.3.2 Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

8.3.3 Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

8.3.4 Enable (\overline{ENx})

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 μ A or 2 μ A when a logic high is present on \overline{EN} . A logic zero input on \overline{EN} restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

8.3.5 Enable (EN)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 μA or 2 μA when a logic low is present on EN. A logic high input on EN restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

8.3.6 Overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{\text{OCx}}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{\text{OCx}}$ is asserted instantaneously.

8.3.7 Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

8.3.8 Thermal Sense

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS204xB-Q1 and TPS205xB-Q1 implement a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

8.3.9 Undervoltage Lockout (UVLO)

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

8.4 Device Functional Modes

Table 8-1 lists OUT pin state as determined by the $\overline{\text{EN}}$ pin.

Table 8-1. OUT Pin State

EN	TPS2041B-Q1	TPS2042B-Q1	TPS2051B-Q1
Low	IN	Open	Open
High	Open	IN	IN

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mbps, or 1.5-Mbps, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts and self-powered hubs (SPHs)
- Bus-powered hubs (BPHs)
- Low-power bus-powered functions
- High-power bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS204xB-Q1 and TPS205xB-Q1 can provide power-distribution solutions to many of these classes of devices.

9.2 Typical Applications

9.2.1 TPS2042B-Q1 Typical Application

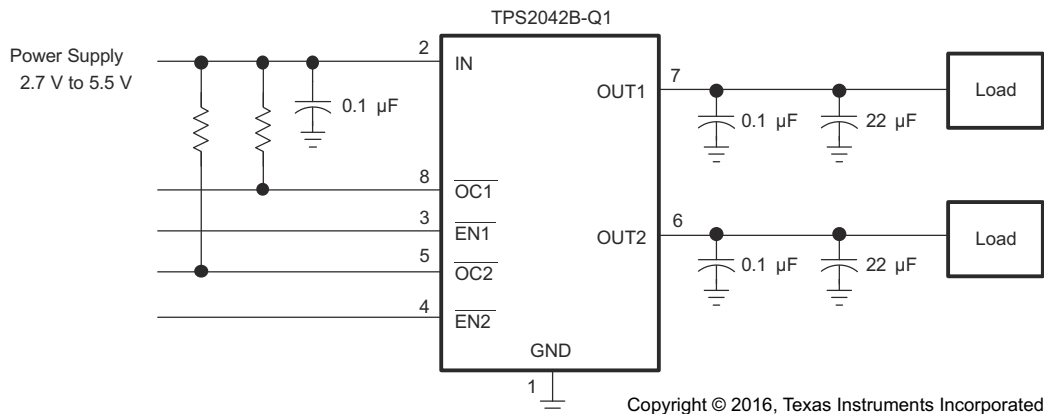


Figure 9-1. Typical Application Schematic Using the TPS2042B-Q1

9.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 9-1](#) as the input parameters.

Table 9-1. Design Parameters

PARAMETER	VALUE
Input voltage	5 V
Output1 voltage	5 V
Output2 voltage	5 V
Output1 current	0.5 A
Output2 current	0.5 A

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

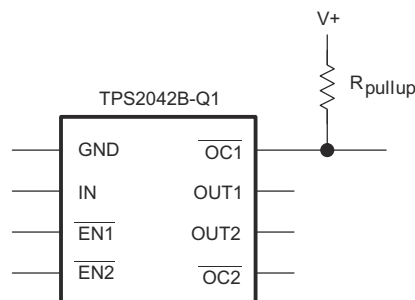
Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see [Figure 9-7](#) through [Figure 9-10](#)). The TPS20xxB-Q1 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see [Figure 6-7](#) through [Figure 6-8](#)). The TPS20xxB-Q1 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

9.2.1.2.2 \overline{OC} Response

The \overline{OCx} open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on \overline{OCx} occurs due to the 10-ms deglitch circuit. The TPS20xxB-Q1 is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. \overline{OCx} is not deglitched when the switch is turned off due to an overtemperature shutdown.



Copyright © 2016, Texas Instruments Incorporated

Figure 9-2. Typical Circuit for the \overline{OC} Pin (TPS2042B-Q1)

9.2.1.3 Application Curves

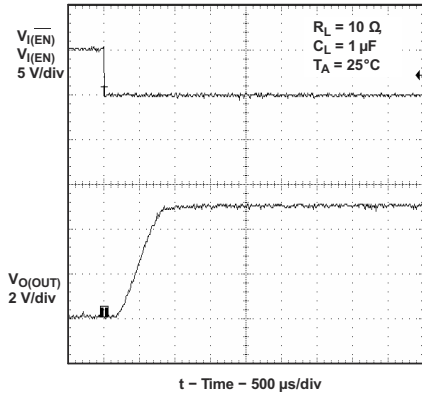


Figure 9-3. Turnon Delay and Rise Time With 1-µF Load

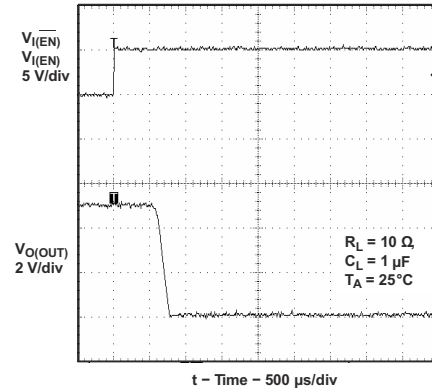


Figure 9-4. Turnoff Delay and Fall Time With 1-µF Load

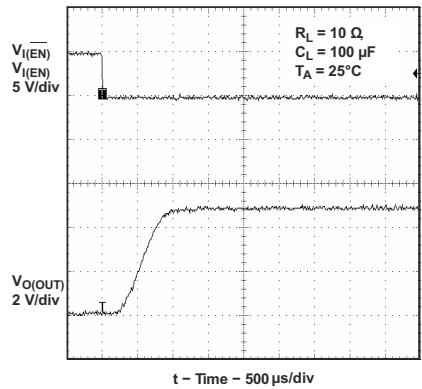


Figure 9-5. Turnon Delay and Rise Time With 100-µF Load

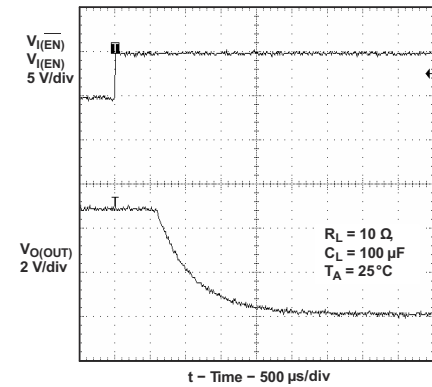


Figure 9-6. Turnoff Delay and Fall Time With 100-µF Load

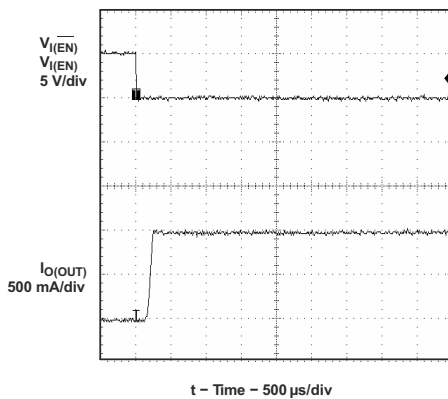


Figure 9-7. Short-Circuit Current, Device Enabled Into Short

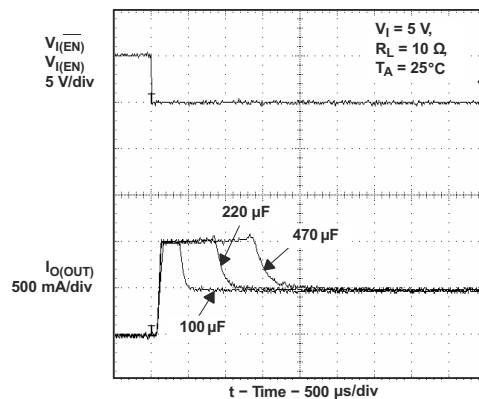
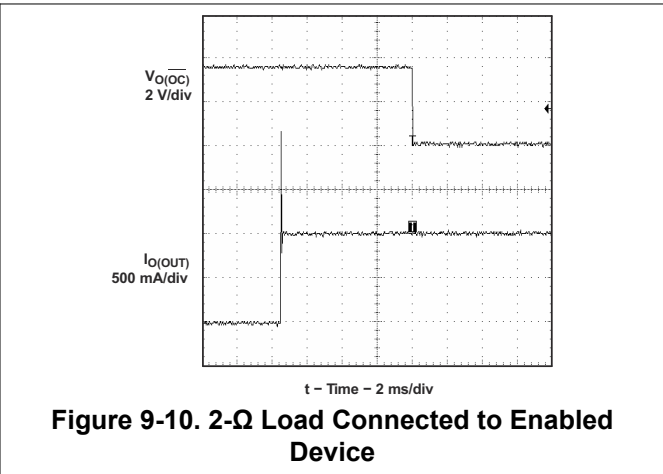
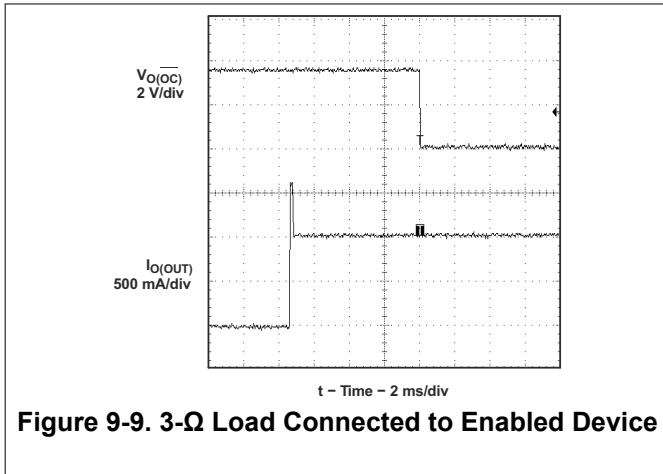


Figure 9-8. Inrush Current With Different Load Capacitance



9.2.2 Hosts and Self-Powered Hubs and Bus-Powered Hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 9-11). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

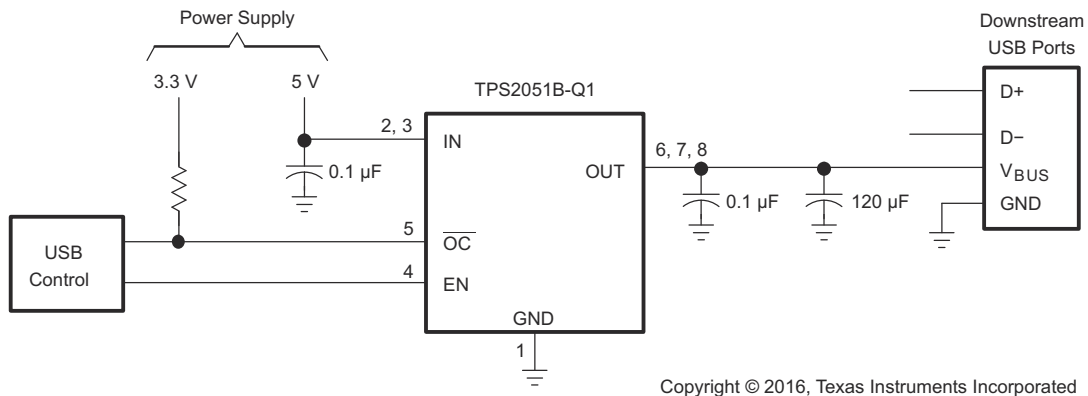


Figure 9-11. Typical One-Port USB Host or Self-Powered Hub

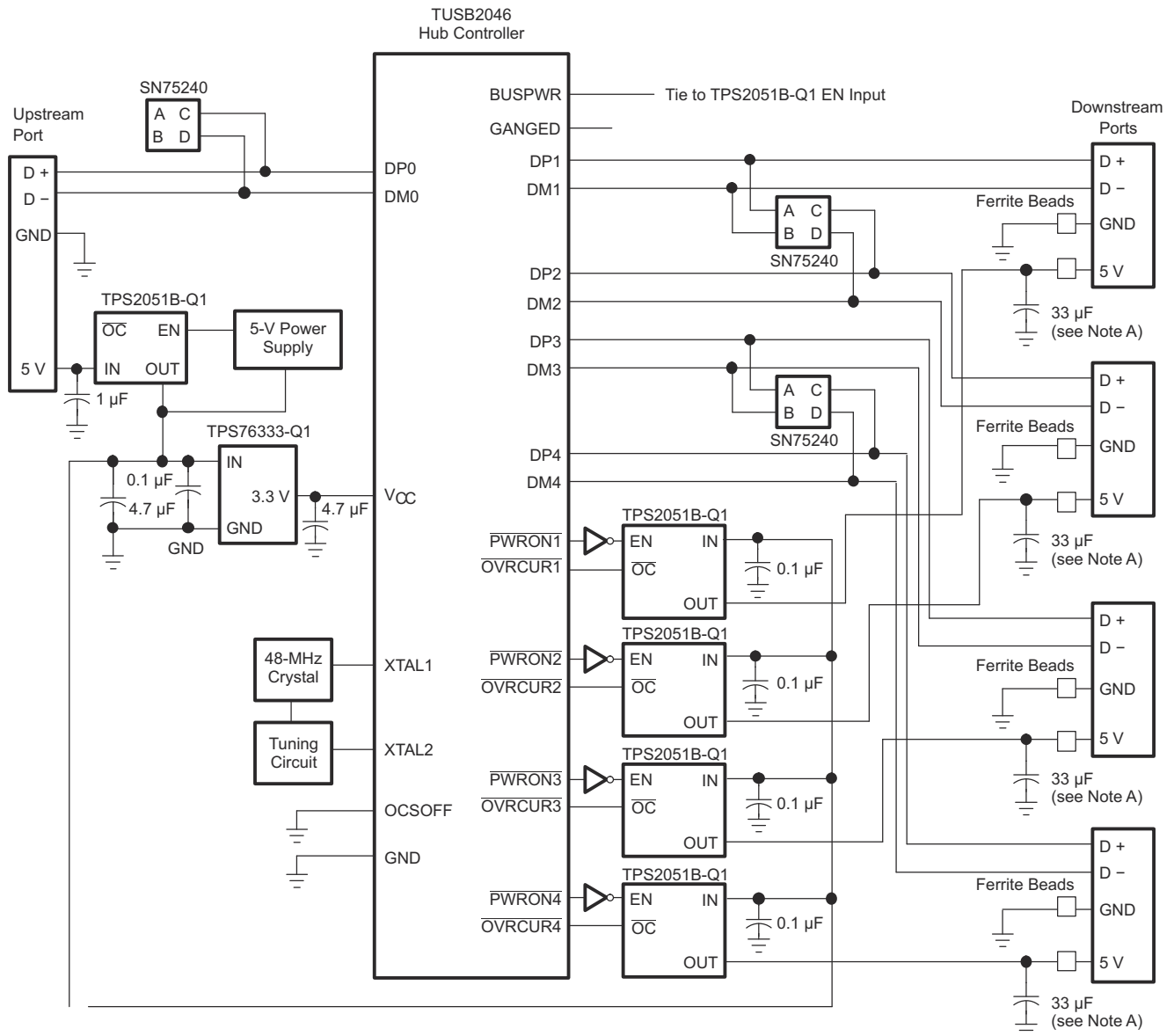
9.2.2.1 Design Requirements

9.2.2.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts and self-powered hubs must:
 - Current-limit downstream ports
 - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
 - Enable and disable power to downstream ports
 - Power up at < 100 mA
 - Limit inrush current (< 44 Ω and 10 μF)
- Functions must:
 - Limit inrush currents
 - Power up at < 100 mA

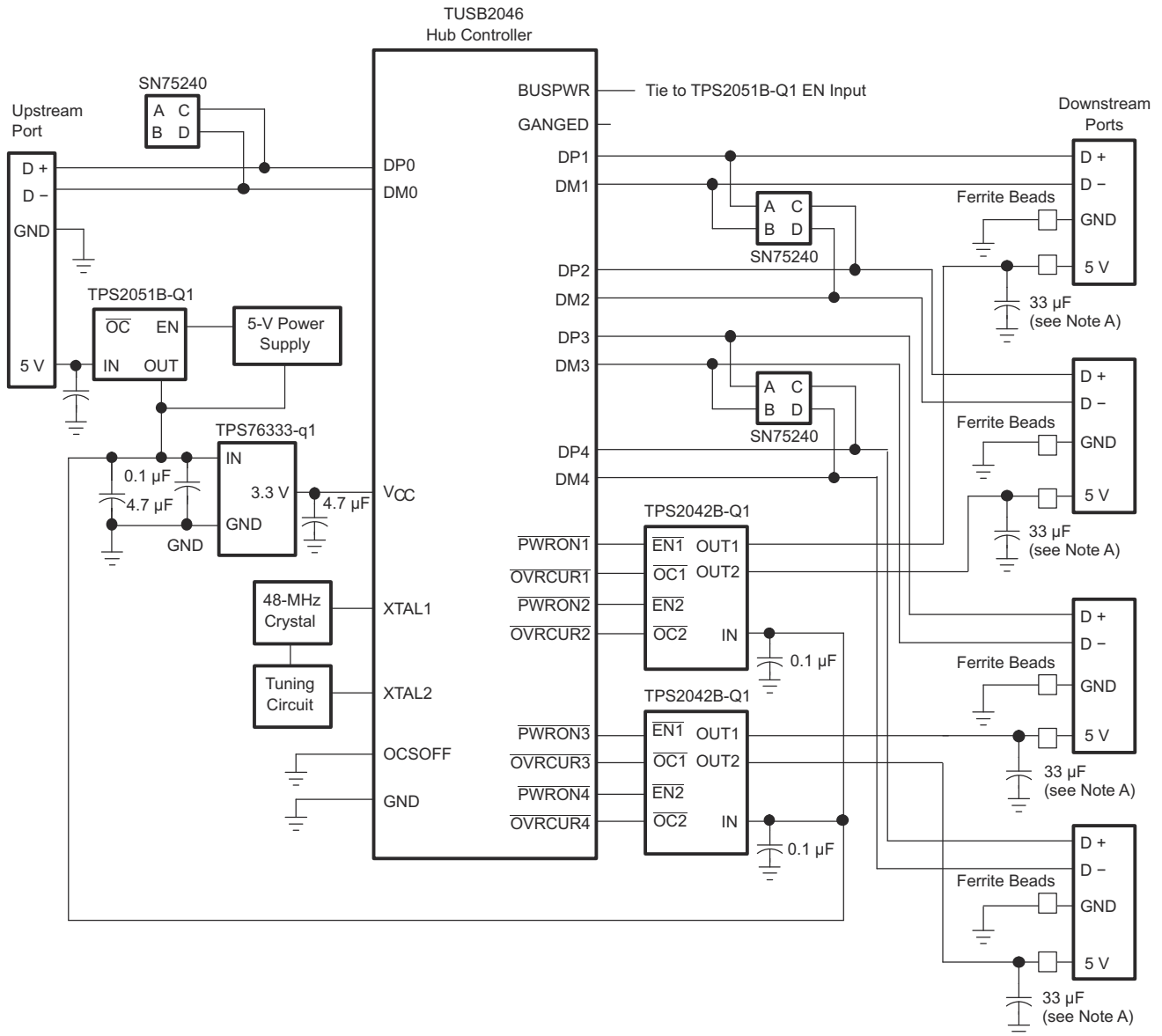
The feature set of the TPS204xB-Q1 and TPS205xB-Q1 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see [Figure 9-12](#) and [Figure 9-13](#)).



Copyright © 2016, Texas Instruments Incorporated

A. USB rev 1.1 requires 120 μF per hub.

Figure 9-12. Hybrid Self-Powered or Bus-Powered Hub Implementation (TPS2051B-Q1)



Copyright © 2016, Texas Instruments Incorporated

A. USB rev 1.1 requires 120 µF per hub.

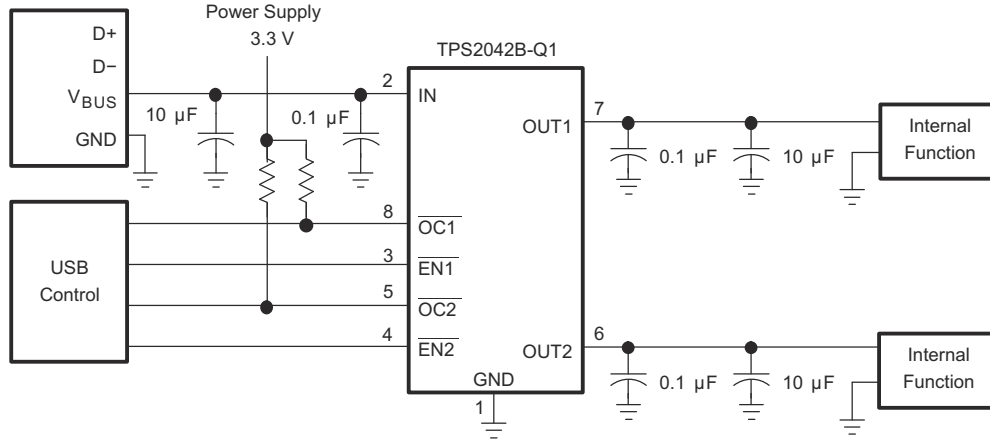
Figure 9-13. Hybrid Self-Powered or Bus-Powered Hub Implementation (TPS2042B-Q1)

9.2.2.2 Detailed Design Procedure

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

9.2.2.2.1 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting (see Figure 9-14).

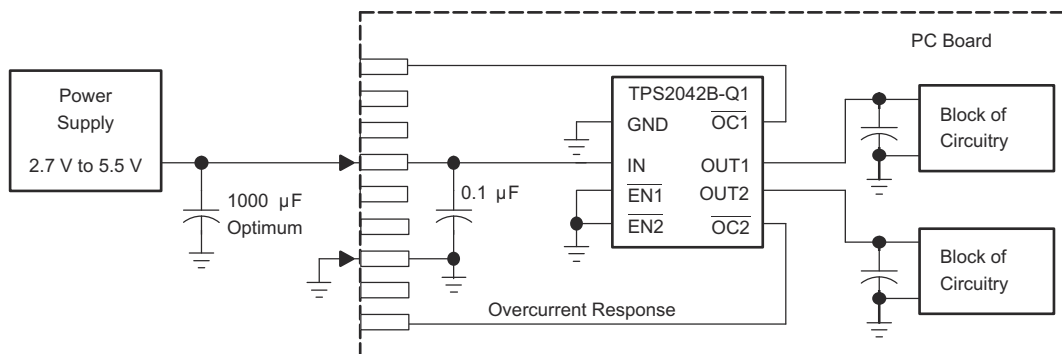


Copyright © 2016, Texas Instruments Incorporated

Figure 9-14. High-Power Bus-Powered Function (TPS2042B-Q1)

9.2.3 Generic Hot-Plug Applications

In many applications, it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise and fall times of the TPS204xB-Q1 and TPS205xB-Q1, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS204xB-Q1 and TPS205xB-Q1 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature ensures a soft start with a controlled rise time for every insertion of the card or module.



Copyright © 2016, Texas Instruments Incorporated

Figure 9-15. Example Hot-Plug Implementation (TPS2042B-Q1)

By placing the TPS204xB-Q1 or TPS205xB-Q1 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

9.2.3.1 Design Requirements

For this design example, use the parameters listed in [Table 9-2](#) as the input parameters.

Table 9-2. Design Parameters

PARAMETER	VALUE
Input voltage	5 V
Output1 voltage	5 V
Output2 voltage	5 V
Output1 current	0.5 A
Output2 current	0.5 A

9.2.3.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer must know the following:

- Normal input operation voltage
- Current limit

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends a 0.1 μ F or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be required on the input to reduce voltage undershoot from exceeding the UVLO of other load share one power rail with TPS2042B-Q1 device or overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply. Output capacitance is not required, but TI recommends placing a high-value electrolytic capacitor on the output pin when large transient currents are expected on the output to reduce the undershoot, which is caused by the inductance of the output power bus just after a short has occurred and the TPS2042B-Q1 device has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges.

10 Power Supply Recommendations

TI recommends a 0.01- μ F to 0.1- μ F ceramic bypass capacitor close to the device between IN and GND. TI recommends placing a high-value electrolytic capacitor on the output pins when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- μ F to 0.1- μ F ceramic capacitor improves the immunity of the device to short-circuit transients. See [Figure 9-1](#).

11 Layout

11.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins and make the connections using a low-inductance trace.
- TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin when large transient currents are expected on the output.

11.2 Layout Example

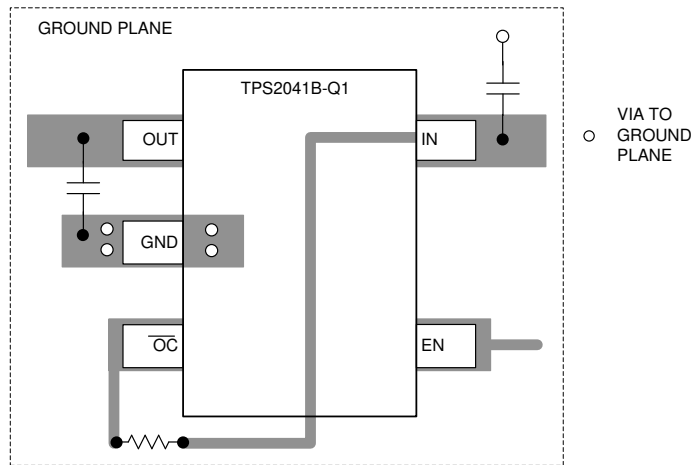


Figure 11-1. Layout Recommendation

11.3 Thermal Considerations

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(ON)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(ON)}$ from [Figure 6-9](#). Using this value, the power dissipation per switch can be calculated by [Equation 1](#):

$$P_D = r_{DS(ON)} \times I^2 \quad (1)$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature with [Equation 2](#):

$$T_J = P_D \times R_{\theta JA} + T_A \quad (2)$$

where

- T_A = Ambient temperature °C
- $R_{\theta JA}$ = Thermal resistance
- P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2041B-Q1	Click here	Click here	Click here	Click here	Click here
TPS2042B-Q1	Click here	Click here	Click here	Click here	Click here
TPS2051B-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2041BQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PLIQ	Samples
TPS2042BQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2042B	Samples
TPS2051BQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2051BQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2041B-Q1, TPS2042B-Q1, TPS2051B-Q1 :

- Catalog: [TPS2041B](#), [TPS2042B](#), [TPS2051B](#)
- Enhanced Product: [TPS2041B-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2041BQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2042BQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TPS2051BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2041BQDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS2042BQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
TPS2051BQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0

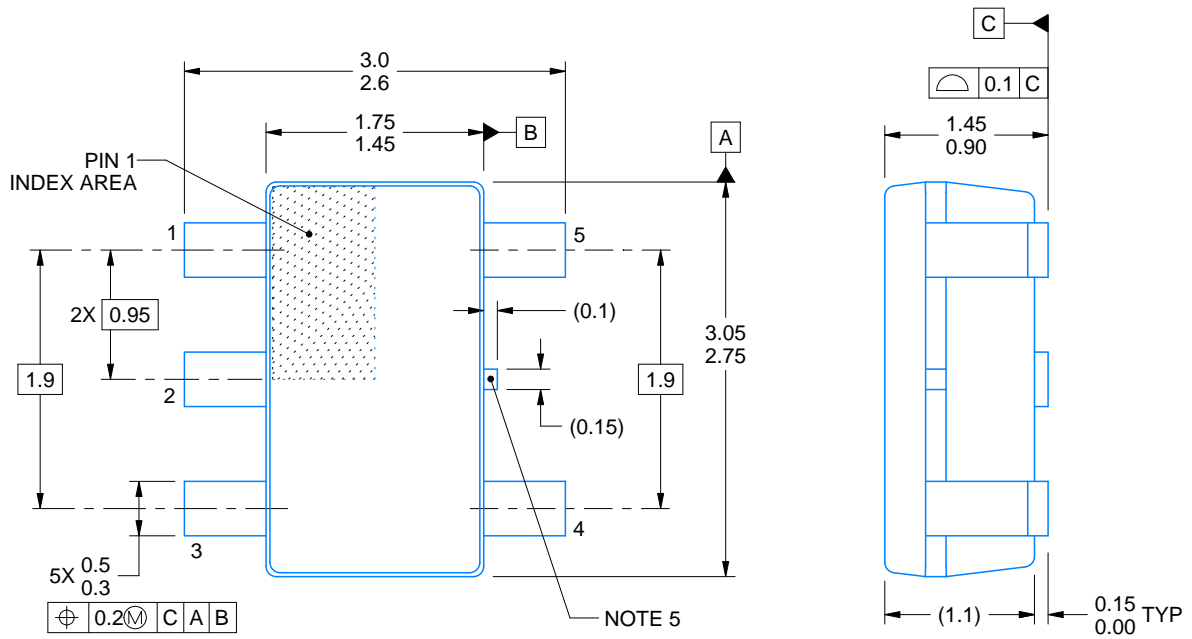
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/G 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

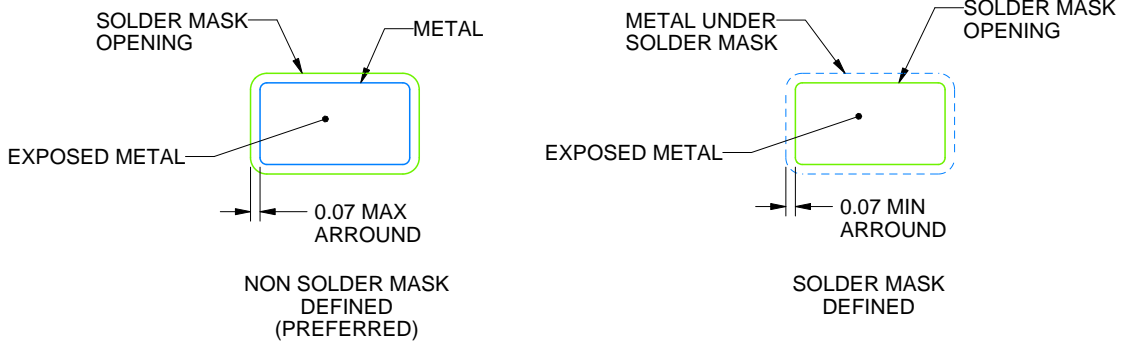
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated