

# NCP1653, NCP1653A

## Controller, PFC, Continuous Conduction Mode, Fixed Frequency, Compact

The NCP1653 is a controller designed for Continuous Conduction Mode (CCM) Power Factor Correction (PFC) boost circuits. It operates in the follower boost or constant output voltage in 67 or 100 kHz fixed switching frequency. Follower boost offers the benefits of reduction of output voltage and hence reduction in the size and cost of the inductor and power switch. Housed in a **PDIP-8** package, the circuit minimizes the number of external components and drastically simplifies the CCM PFC implementation. It also integrates high safety protection features. The NCP1653 is a driver for robust and compact PFC stages.

### Features

- IEC1000-3-2 Compliant
- Continuous Conduction Mode
- Average Current-Mode or Peak Current-Mode Operation
- Constant Output Voltage or Follower Boost Operation
- Very Few External Components
- Fixed Switching Frequency: 67 kHz = NCP1653A, 100 kHz = NCP1653
- Soft-Start Capability
- $V_{CC}$  Undervoltage Lockout with Hysteresis (8.7 / 13.25 V)
- Overvoltage Protection (107% of Nominal Output Level)
- Undervoltage Protection or Shutdown (8% of Nominal Output Level)
- Programmable Overcurrent Protection
- Programmable Overpower Limitation
- Thermal Shutdown with Hysteresis (120 / 150°C)
- This is a Pb-Free Device

### Typical Applications

- TV & Monitors
- PC Desktop SMPS
- AC Adapters SMPS
- White Goods

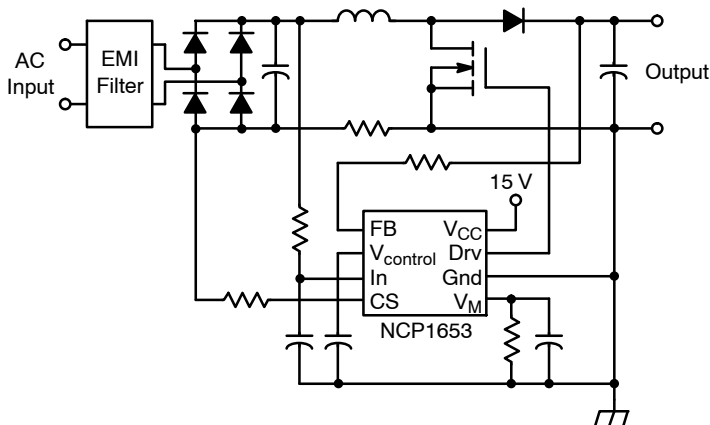


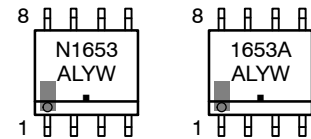
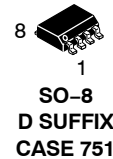
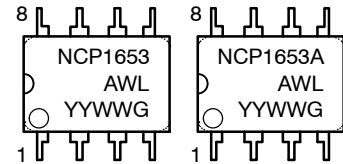
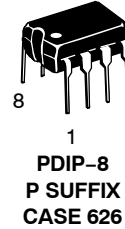
Figure 1. Typical Application Circuit



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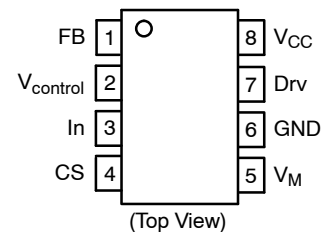
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### MARKING DIAGRAMS



A suffix = 67 kHz option  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

# NCP1653, NCP1653A

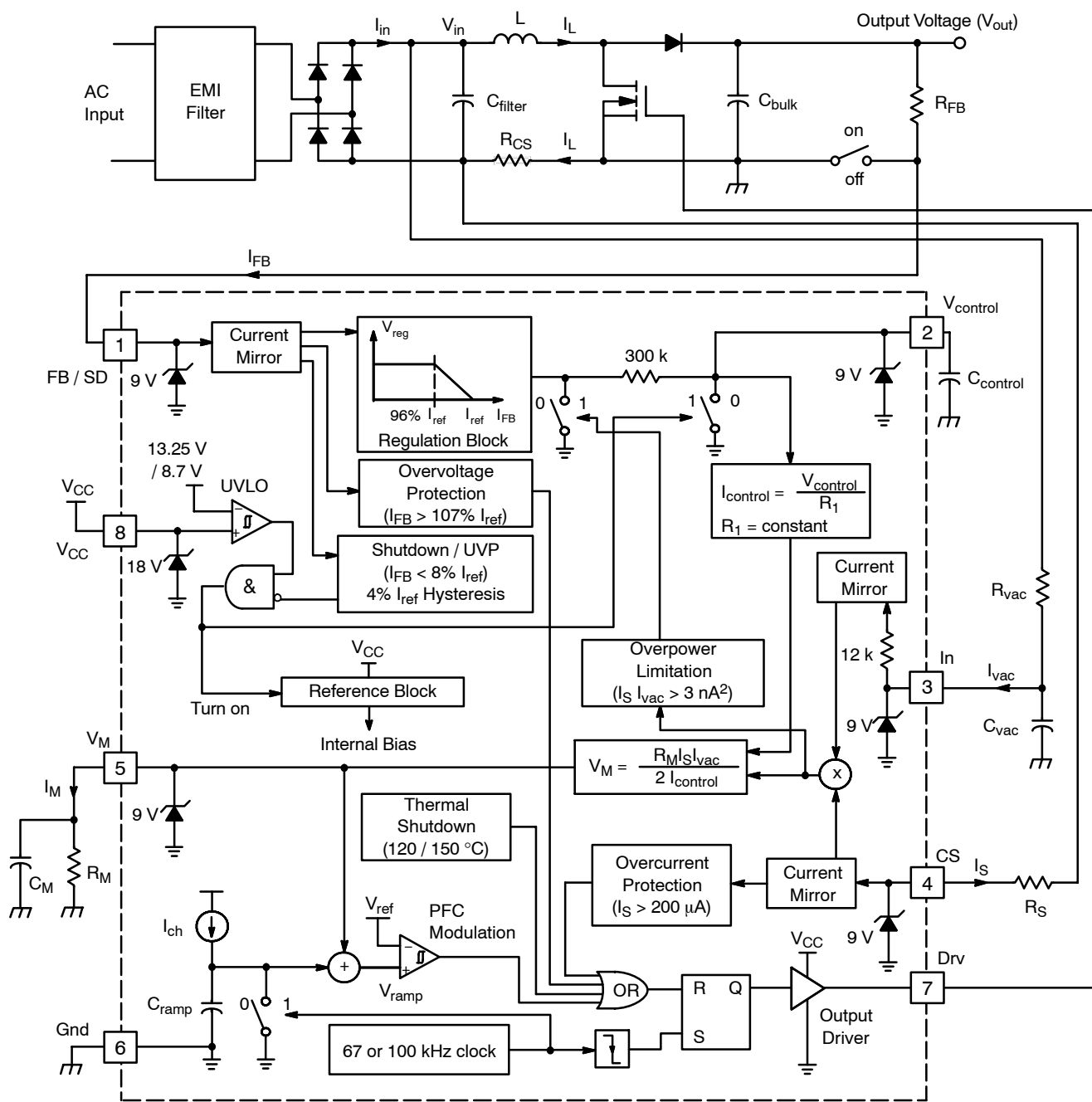


Figure 2. Functional Block Diagram

# NCP1653, NCP1653A

## PIN FUNCTION DESCRIPTION

Pin	Symbol	Name	Function
1	FB / SD	Feedback / Shutdown	This pin receives a feedback current $I_{FB}$ which is proportional to the PFC circuit output voltage. The current is for output regulation, output overvoltage protection (OVP), and output undervoltage protection (UVP). When $I_{FB}$ goes above 107% $I_{ref}$ , OVP is activated and the Drive Output is disabled. When $I_{FB}$ goes below 8% $I_{ref}$ , the device enters a low-consumption shutdown mode.
2	$V_{control}$	Control Voltage / Soft-Start	The voltage of this pin $V_{control}$ directly controls the input impedance and hence the power factor of the circuit. This pin is connected to an external capacitor $C_{control}$ to limit the $V_{control}$ bandwidth typically below 20 Hz to achieve near unity power factor. The device provides no output when $V_{control} = 0$ V. Hence, $C_{control}$ also works as a soft-start capacitor.
3	In	Input Voltage Sense	This pin sinks an input-voltage current $I_{vac}$ which is proportional to the RMS input voltage $V_{ac}$ . The current $I_{vac}$ is for overpower limitation (OPL) and PFC duty cycle modulation. When the product ( $I_S \cdot I_{vac}$ ) goes above 3 nA <sup>2</sup> , OPL is activated and the Drive Output duty ratio is reduced by pulling down $V_{control}$ indirectly to reduce the input power.
4	CS	Input Current Sense	This pin sources a current $I_S$ which is proportional to the inductor current $I_L$ . The sense current $I_S$ is for overcurrent protection (OCP), overpower limitation (OPL) and PFC duty cycle modulation. When $I_S$ goes above 200 $\mu$ A, OCP is activated and the Drive Output is disabled.
5	$V_M$	Multiplier Voltage	This pin provides a voltage $V_M$ for the PFC duty cycle modulation. The input impedance of the PFC circuit is proportional to the resistor $R_M$ externally connected to this pin. The device operates in average current-mode if an external capacitor $C_M$ is connected to the pin. Otherwise, it operates in peak current-mode.
6	GND	The IC Ground	-
7	Drv	Drive Output	This pin provides an output to an external MOSFET.
8	$V_{CC}$	Supply Voltage	This pin is the positive supply of the device. The operating range is between 8.75 V and 18 V with UVLO start threshold 13.25 V.

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
FB, $V_{control}$ , In, CS, $V_M$ Pins (Pins 1–5) Maximum Voltage Range Maximum Current	$V_{max}$ $I_{max}$	-0.3 to +9 100	V mA
Drive Output (Pin 7) Maximum Voltage Range Maximum Current Range (Note 3)	$V_{max}$ $I_{max}$	-0.3 to +18 1.5	V A
Power Supply Voltage (Pin 8) Maximum Voltage Range Maximum Current	$V_{max}$ $I_{max}$	-0.3 to +18 100	V mA
Transient Power Supply Voltage, Duration < 10 ms, $I_{VCC} < 20$ mA		25	V
Power Dissipation and Thermal Characteristics P suffix, Plastic Package, Case 626 Maximum Power Dissipation @ $T_A = 70^\circ\text{C}$ Thermal Resistance Junction-to-Air D suffix, Plastic Package, Case 751 Maximum Power Dissipation @ $T_A = 70^\circ\text{C}$ Thermal Resistance Junction-to-Air	$P_D$ $R_{\theta JA}$ $P_D$ $R_{\theta JA}$	800 100 450 178	mW $^\circ\text{C/W}$ mW $^\circ\text{C/W}$
Operating Junction Temperature Range	$T_J$	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:  
Pins 1–8: Human Body Model 2000 V per JEDEC Standard JESD22, Method A114.  
Machine Model Method 190 V per JEDEC Standard JES222, Method A115A.
- This device contains Latchup protection and exceeds  $\pm 100$  mA per JEDEC Standard JESD78.
- Guaranteed by design.

# NCP1653, NCP1653A

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ . For min/max values,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 15\text{ V}$ ,  $I_{FB} = 100\ \mu\text{A}$ ,  $I_{vac} = 30\ \mu\text{A}$ ,  $I_S = 0\ \mu\text{A}$ , unless otherwise specified)

Characteristics	Pin	Symbol	Min	Typ	Max	Unit	
<b>OSCILLATOR</b>							
Switching Frequency	NCP1653 NCP1653A	7	$f_{sw}$	90 60.3	102 67	110 73.7	kHz
Maximum Duty Cycle ( $V_M = 0\text{ V}$ ) (Note 3)		7	$D_{max}$	94	–	–	%
<b>GATE DRIVE</b>							
Gate Drive Resistor		7					
Output High and Draw 100 mA out of Drv pin ( $I_{source} = 100\text{ mA}$ )			$R_{OH}$	5.0	9.0	20	$\Omega$
Output Low and Insert 100 mA into Drv pin ( $I_{sink} = 100\text{ mA}$ )			$R_{OL}$	2.0	6.6	18	$\Omega$
Gate Drive Rise Time from 1.5 V to 13.5 V (Drv = 2.2 nF to Gnd)		7	$t_r$	–	88	–	ns
Gate Drive Fall Time from 13.5 V to 1.5 V (Drv = 2.2 nF to Gnd)		7	$t_f$	–	61.5	–	ns
<b>FEEDBACK / OVERVOLTAGE PROTECTION / UNDERVOLTAGE PROTECTION</b>							
Reference Current ( $V_M = 3\text{ V}$ )		1	$I_{ref}$	192	204	208	$\mu\text{A}$
Regulation Block Ratio		1	$I_{regL}/I_{ref}$	95	96	98	%
Vcontrol Pin Internal Resistor		2	$R_{control}$	–	300	–	k $\Omega$
Maximum Control Voltage ( $I_{FB} = 100\ \mu\text{A}$ )		2	$V_{control(max)}$	–	2.4	–	V
Maximum Control Current ( $I_{control(max)} = I_{ref} / 2$ )		2	$I_{control(max)}$	–	100	–	$\mu\text{A}$
Feedback Pin Voltage ( $I_{FB} = 100\ \mu\text{A}$ )		1	$V_{FB1}$	1.0	1.5	1.9	V
Feedback Pin Voltage ( $I_{FB} = 200\ \mu\text{A}$ )				1.3	1.8	2.2	V
Overvoltage Protection		1					
OVP Ratio			$I_{OVP}/I_{ref}$	104	107	–	%
Current Threshold			$I_{OVP}$	–	214	230	$\mu\text{A}$
Propagation Delay			$t_{OVP}$	–	500	–	ns
Undervoltage Protection ( $V_M = 3\text{ V}$ )		1					
UVP Activate Threshold Ratio			$I_{UVP(on)}/I_{ref}$	4.0	8.0	15	%
UVP Deactivate Threshold Ratio			$I_{UVP(off)}/I_{ref}$	7.0	12	20	%
UVP Lockout Hysteresis			$I_{UVP(H)}$	4.0	8.0	–	$\mu\text{A}$
Propagation Delay			$t_{UVP}$	–	500	–	ns
<b>CURRENT SENSE</b>							
Current Sense Pin Offset Voltage ( $I_S = 100\ \mu\text{A}$ )		4	$V_S$	0	10	30	mV
Overcurrent Protection Threshold ( $V_M = 1\text{ V}$ )		4	$I_S(OCP)$	185	200	215	$\mu\text{A}$
<b>OVERPOWER LIMITATION</b>							
Input Voltage Sense Pin Internal Resistor		4	$R_{vac(int)}$	–	12	–	k $\Omega$
Over Power Limitation Threshold		3–4	$I_S \times I_{vac}$	–	3.0	–	nA <sup>2</sup>
Sense Current Threshold ( $I_{vac} = 30\ \mu\text{A}$ , $V_M = 3\text{ V}$ )		4	$I_S(OPL1)$	80	100	140	$\mu\text{A}$
Sense Current Threshold ( $I_{vac} = 100\ \mu\text{A}$ , $V_M = 3\text{ V}$ )			$I_S(OPL2)$	24	32	48	$\mu\text{A}$
<b>CURRENT MODULATION</b>							
PWM Comparator Reference Voltage		5	$V_{ref}$	2.25	2.62	2.75	V
Multiplier Current ( $V_{control} = V_{control(max)}$ , $I_{vac} = 30\ \mu\text{A}$ , $I_S = 25\ \mu\text{A}$ )		5	$I_{M1}$	1.0	2.85	5.8	$\mu\text{A}$
Multiplier Current ( $V_{control} = V_{control(max)}$ , $I_{vac} = 30\ \mu\text{A}$ , $I_S = 75\ \mu\text{A}$ )			$I_{M2}$	3.2	9.5	18	$\mu\text{A}$
Multiplier Current ( $V_{control} = V_{control(max)} / 10$ , $I_{vac} = 30\ \mu\text{A}$ , $I_S = 25\ \mu\text{A}$ )			$I_{M3}$	10	35	58	$\mu\text{A}$
Multiplier Current ( $V_{control} = V_{control(max)} / 10$ , $I_{vac} = 30\ \mu\text{A}$ , $I_S = 75\ \mu\text{A}$ )			$I_{M4}$	30	103.5	180	$\mu\text{A}$
<b>THERMAL SHUTDOWN</b>							
Thermal Shutdown Threshold (Note 4)		–	$T_{SD}$	150	–	–	$^\circ\text{C}$
Thermal Shutdown Hysteresis		–	–	–	30	–	$^\circ\text{C}$

4. Guaranteed by design.

# NCP1653, NCP1653A

**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ . For min/max values,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 15\text{ V}$ ,  $I_{FB} = 100\ \mu\text{A}$ ,  $I_{vac} = 30\ \mu\text{A}$ ,  $I_S = 0\ \mu\text{A}$ , unless otherwise specified)

Characteristics	Pin	Symbol	Min	Typ	Max	Unit
<b>SUPPLY SECTION</b>						
Supply Voltage	8					
UVLO Startup Threshold		$V_{CC(on)}$	12.25	13.25	14.5	V
Minimum Operating Voltage after Startup		$V_{CC(off)}$	8.0	8.7	9.5	V
UVLO Hysteresis		$V_{CC(H)}$	4.0	4.55	–	V
Supply Current:	8					
Startup ( $V_{CC} = V_{CC(on)} - 0.2\text{ V}$ )		$I_{stup}$	–	18	50	$\mu\text{A}$
Startup ( $V_{CC} < 8.0\text{ V}$ , $I_{FB} = 200\ \mu\text{A}$ )		$I_{stup1}$	–	0.95	1.5	mA
Startup ( $8.0\text{ V} < V_{CC} < V_{CC(on)} - 0.2\text{ V}$ , $I_{FB} = 200\ \mu\text{A}$ )		$I_{stup2}$	–	21	50	$\mu\text{A}$
Startup ( $V_{CC} < V_{CC(on)} - 0.2\text{ V}$ , $I_{FB} = 0\ \mu\text{A}$ ) (Note 5)		$I_{stup3}$	–	21	50	$\mu\text{A}$
Operating ( $V_{CC} = 15\text{ V}$ , Drv = open, $V_M = 3\text{ V}$ )		$I_{CC1}$	–	3.7	5.0	mA
Operating ( $V_{CC} = 15\text{ V}$ , Drv = 1 nF to Gnd, $V_M = 1\text{ V}$ )		$I_{CC2}$	–	4.7	6.0	mA
Shutdown ( $V_{CC} = 15\text{ V}$ and $I_{FB} = 0\text{ A}$ )		$I_{stdn}$	–	33	50	$\mu\text{A}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Please refer to the “Biasing the Controller” Section in the Functional Description.

# NCP1653, NCP1653A

## TYPICAL CHARACTERISTICS

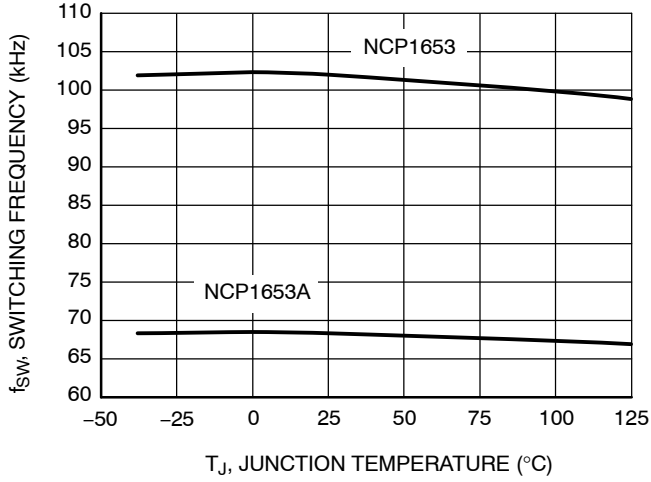


Figure 3. Switching Frequency vs. Temperature

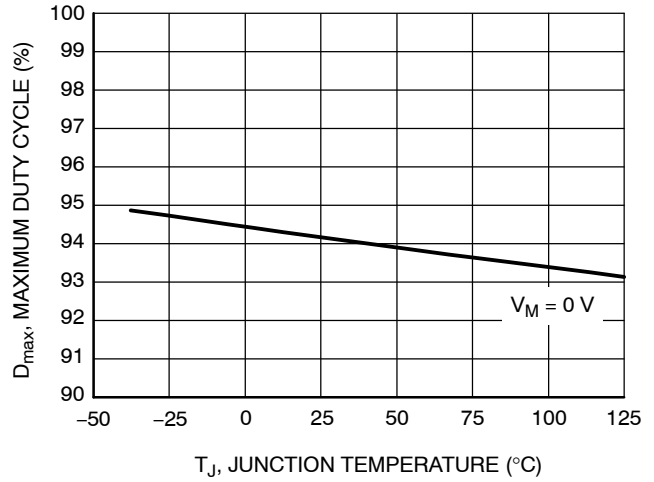


Figure 4. Maximum Duty Cycle vs. Temperature

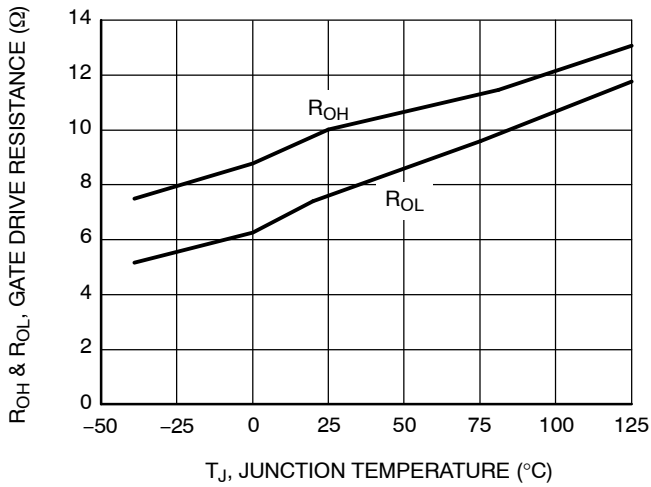


Figure 5. Gate Drive Resistance vs. Temperature

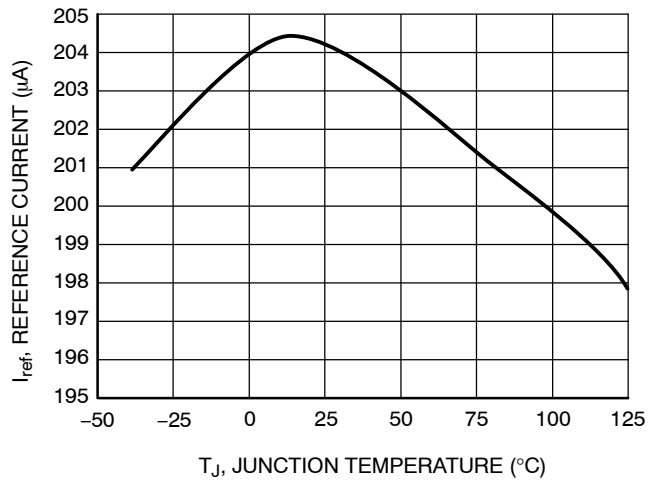


Figure 6. Reference Current vs. Temperature

# NCP1653, NCP1653A

## TYPICAL CHARACTERISTICS

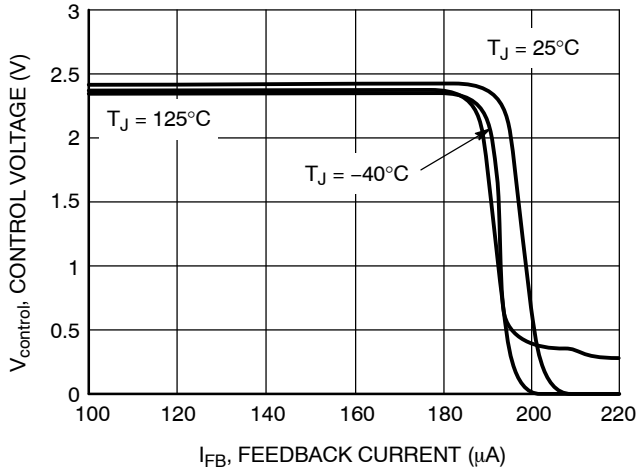


Figure 7. Regulation Block

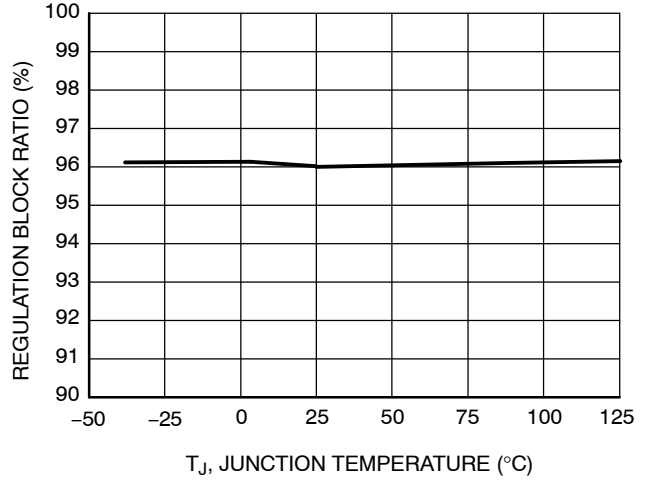


Figure 8. Regulation Block Ratio vs. Temperature

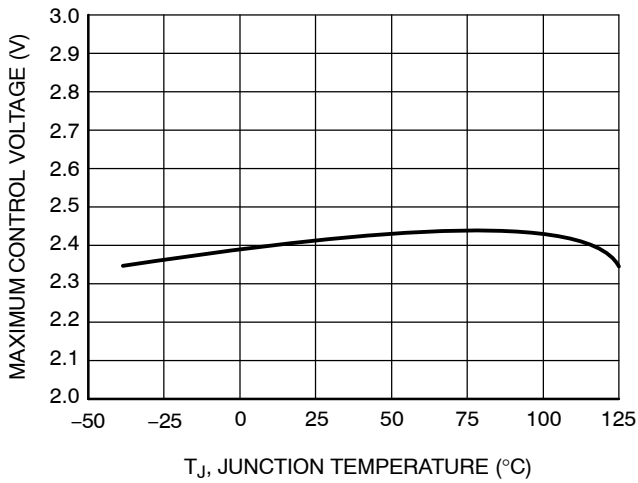


Figure 9. Maximum Control Voltage vs. Temperature

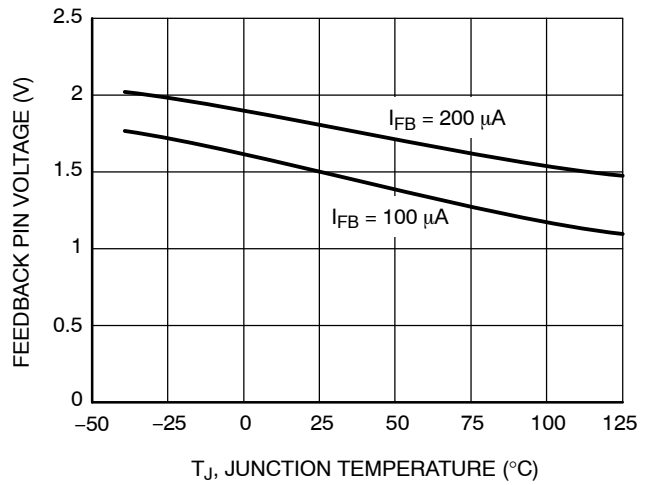


Figure 10. Feedback Pin Voltage vs. Temperature

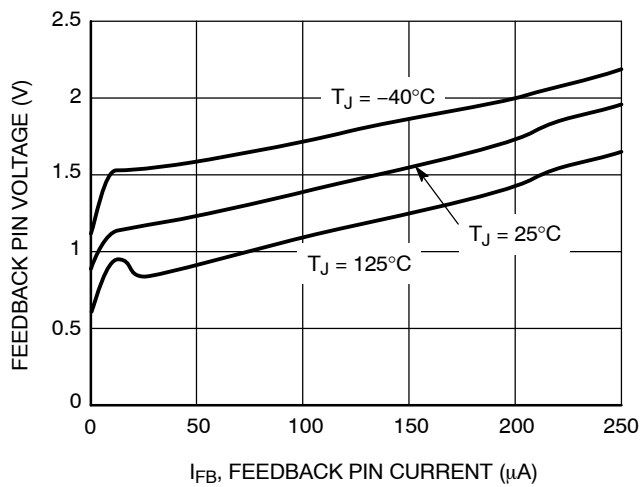


Figure 11. Feedback Pin Voltage vs. Feedback Current

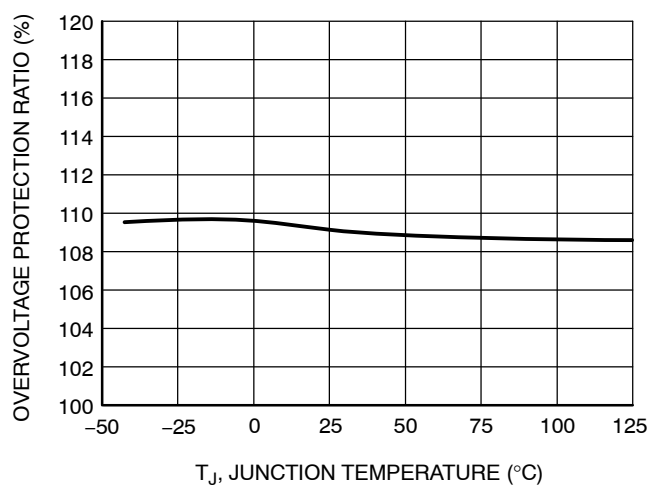


Figure 12. Overvoltage Protection Ratio vs. Temperature

TYPICAL CHARACTERISTICS

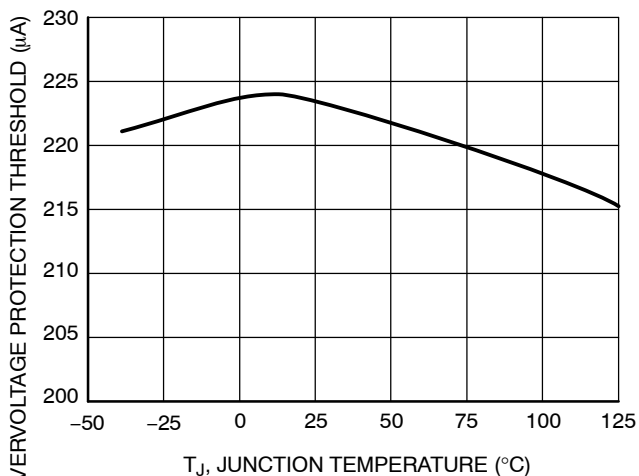


Figure 13. Overvoltage Protection Threshold vs. Temperature

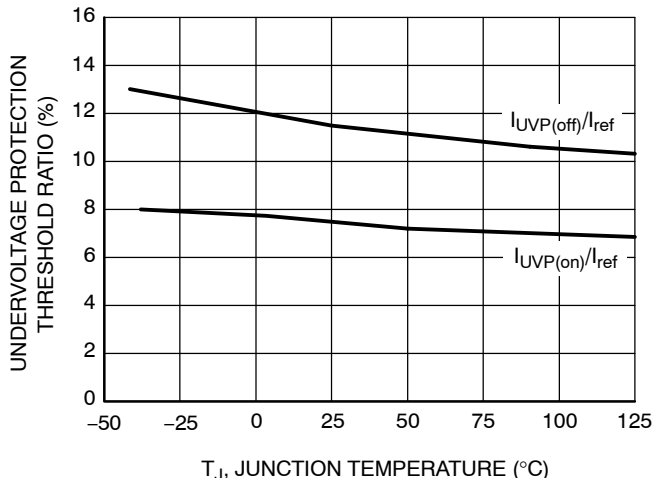


Figure 14. Undervoltage Protection Thresholds vs. Temperature

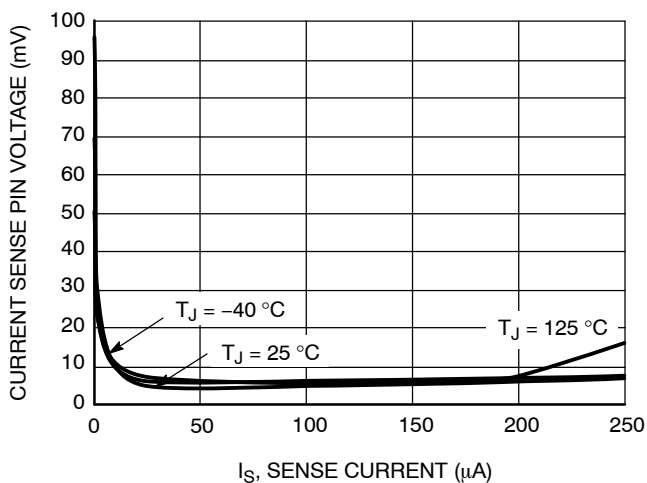


Figure 15. Current Sense Pin Voltage vs. Sense Current

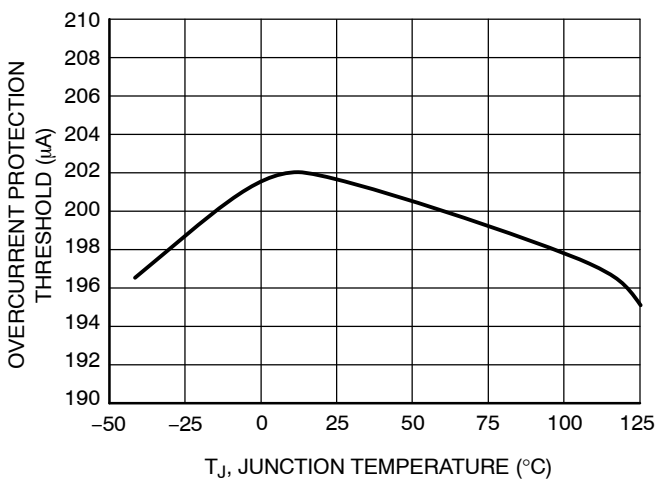


Figure 16. Overcurrent Protection Threshold vs. Temperature

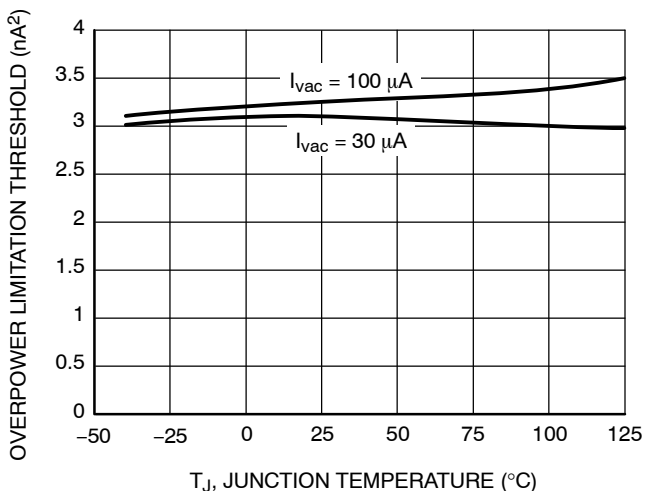


Figure 17. Overpower Limitation Threshold vs. Temperature

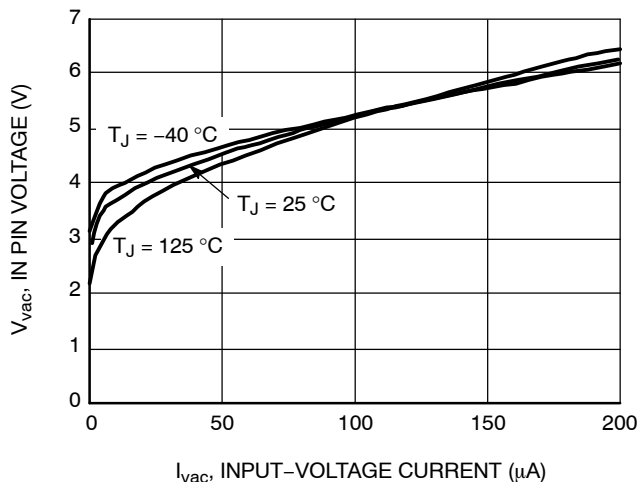
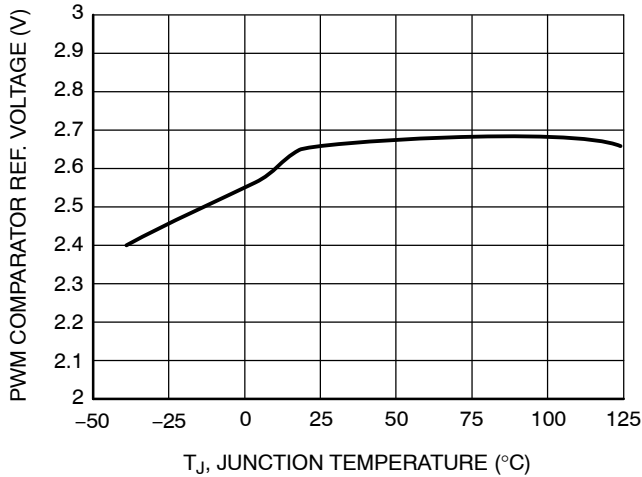


Figure 18. In Pin Voltage vs. Input-Voltage Current

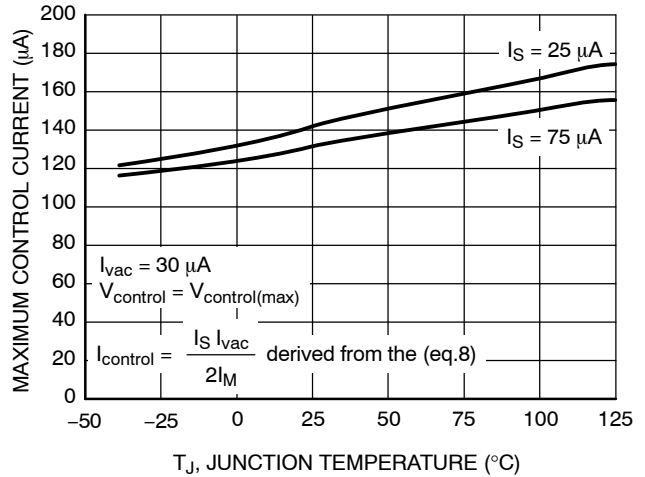


# NCP1653, NCP1653A

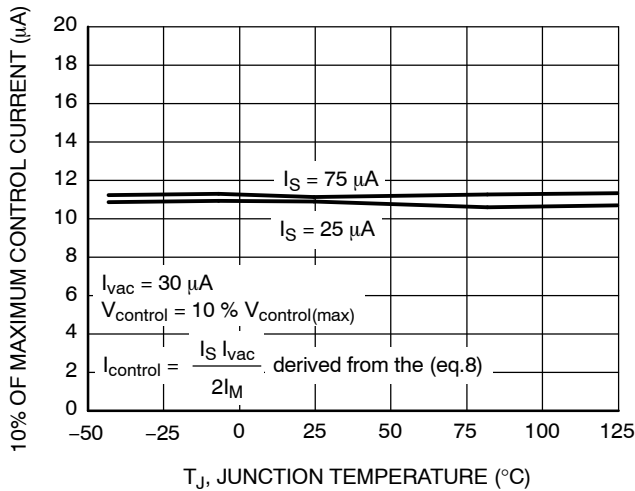
## TYPICAL CHARACTERISTICS



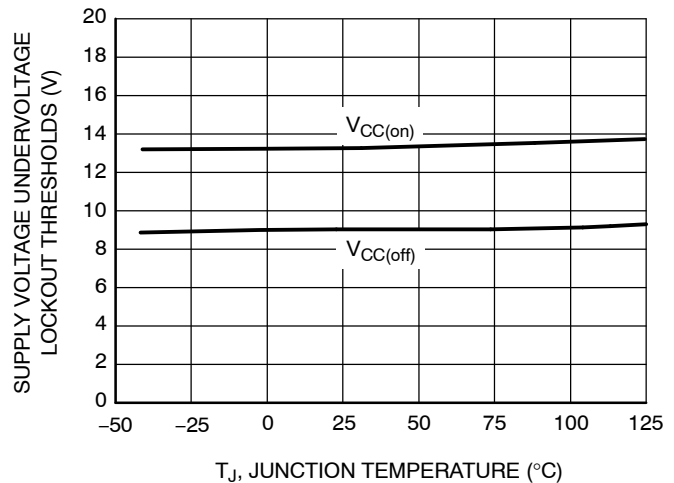
**Figure 19. PWM Comparator Reference Voltage vs. Temperature**



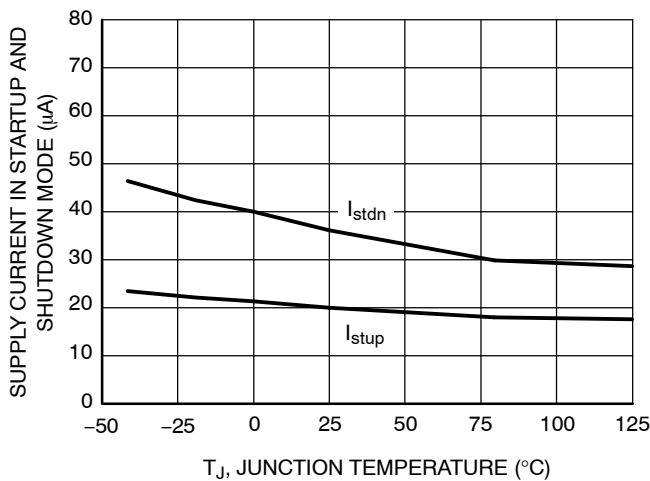
**Figure 20. Maximum Control Current vs. Temperature**



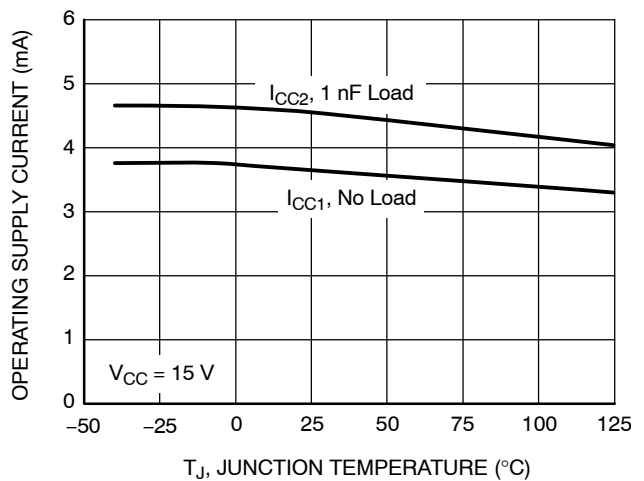
**Figure 21. 10% of Maximum Control Current vs. Temperature**



**Figure 22. Supply Voltage Undervoltage Lockout Thresholds vs. Temperature**



**Figure 23. Supply Current in Startup and Shutdown Mode vs. Temperature**



**Figure 24. Operating Supply Current vs. Temperature**

## FUNCTIONAL DESCRIPTION

### Introduction

The NCP1653 is a Power Factor Correction (PFC) boost controller designed to operate in fixed-frequency Continuous Conduction Mode (CCM). It can operate in either peak current-mode or average current-mode.

Fixed-frequency operation eases the compliance with EMI standards and the limitation of the possible radiated noise that may pollute surrounding systems. The CCM operation reduces the application di/dt and the resulting interference. The NCP1653 is designed in a compact 8-pin package which offers the minimum number of external components. It simplifies the design and reduces the cost. The output stage of the NCP1653 incorporates  $\pm 1.5$  A current capability for direct driving of the MOSFET in high-power applications.

The NCP1653 is implemented in constant output voltage or follower boost modes. The follower boost mode permits one to significantly reduce the size of the PFC circuit inductor and power MOSFET. With this technique, the output voltage is not set at a constant level but depends on the RMS input voltage or load demand. It allows lower output voltage and hence the inductor and power MOSFET size or cost are reduced.

Hence, NCP1653 is an ideal candidate in high-power applications where cost-effectiveness, reliability and high power factor are the key parameters. The NCP1653 incorporates all the necessary features to build a compact and rugged PFC stage.

The NCP1653 provides the following protection features:

1. **Overvoltage Protection (OVP)** is activated and the Drive Output (Pin 7) goes low when the output voltage exceeds 107% of the nominal regulation level which is a user-defined value. The circuit automatically resumes operation when the output voltage becomes lower than the 107%.
2. **Undervoltage Protection (UVP)** is activated and the device is shut down when the output voltage goes below 8% of the nominal regulation level. The circuit automatically starts operation when the output voltage goes above 12% of the nominal regulation level. This feature also provides output open-loop protection, and an external shutdown feature.
3. **Overpower Limitation (OPL)** is activated and the Drive Output (Pin 7) duty ratio is reduced by pulling down an internal signal when a computed input power exceeds a permissible level. OPL is automatically deactivated when this computed input power becomes lower than the permissible level.
4. **Overcurrent Protection (OCP)** is activated and the Drive Output (Pin 7) goes low when the inductor current exceeds a user-defined value. The operation resumes when the inductor current becomes lower than this value.

5. **Thermal Shutdown (TSD)** is activated and the Drive Output (Pin 7) is disabled when the junction temperature exceeds  $150^{\circ}\text{C}$ . The operation resumes when the junction temperature falls down by typical  $30^{\circ}\text{C}$ .

### CCM PFC Boost

A CCM PFC boost converter is shown in Figure 25. The input voltage is a rectified 50 or 60 Hz sinusoidal signal. The MOSFET is switching at a high frequency (typically 102 kHz in the NCP1653) so that the inductor current  $I_L$  basically consists of high and low-frequency components.

Filter capacitor  $C_{\text{filter}}$  is an essential and very small value capacitor in order to eliminate the high-frequency component of the inductor current  $I_L$ . This filter capacitor cannot be too bulky because it can pollute the power factor by distorting the rectified sinusoidal input voltage.

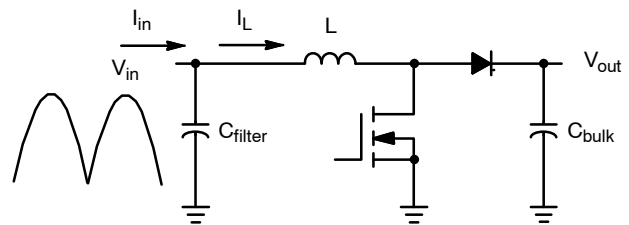


Figure 25. CCM PFC Boost Converter

### PFC Methodology

The NCP1653 uses a proprietary PFC methodology particularly designed for CCM operation. The PFC methodology is described in this section.

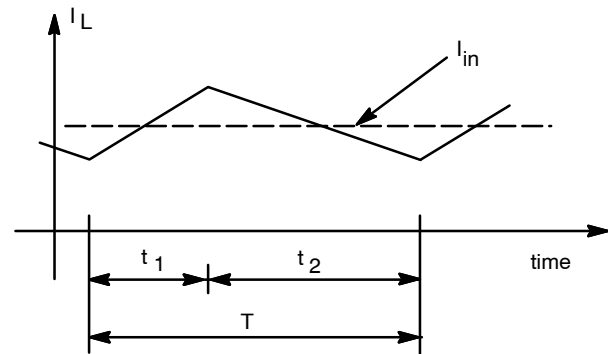


Figure 26. Inductor Current in CCM

As shown in Figure 26, the inductor current  $I_L$  in a switching period  $T$  includes a charging phase for duration  $t_1$  and a discharging phase for duration  $t_2$ . The voltage conversion ratio is obtained in (eq.1).

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_1 + t_2}{t_2} = \frac{T}{T - t_1}$$

$$V_{\text{in}} = \frac{T - t_1}{T} V_{\text{out}} \quad (\text{eq.1})$$

The input filter capacitor  $C_{\text{filter}}$  and the front-ended EMI filter absorbs the high-frequency component of inductor current  $I_L$ . It makes the input current  $I_{\text{in}}$  a low-frequency signal only of the inductor current.

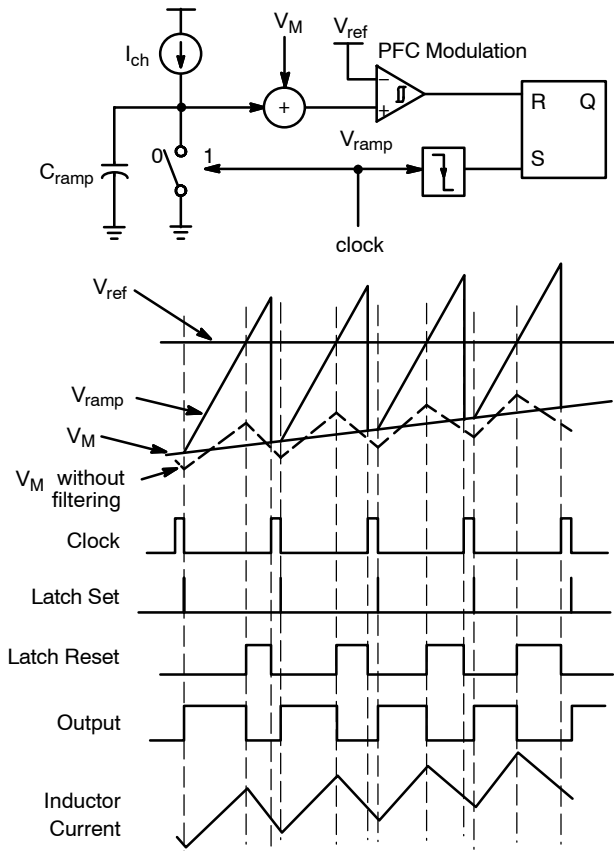
$$I_{\text{in}} = I_{L-50} \quad (\text{eq.2})$$

The suffix 50 means it is with a 50 or 60 Hz bandwidth of the original  $I_L$ .

From (eq.1) and (eq.2), the input impedance  $Z_{\text{in}}$  is formulated.

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{T - t_1}{T} \frac{V_{\text{out}}}{I_{L-50}} \quad (\text{eq.3})$$

Power factor is corrected when the input impedance  $Z_{\text{in}}$  in (eq.3) is constant or slowly varying in the 50 or 60 Hz bandwidth.



**Figure 27. PFC Duty Modulation and Timing Diagram**

The PFC duty modulation and timing diagram is shown in Figure 27. The MOSFET on time  $t_1$  is generated by the intersection of reference voltage  $V_{\text{ref}}$  and ramp voltage  $V_{\text{ramp}}$ . A relationship in (eq.4) is obtained.

$$V_{\text{ramp}} = V_M + \frac{I_{\text{ch}} t_1}{C_{\text{ramp}}} = V_{\text{ref}} \quad (\text{eq.4})$$

The charging current  $I_{\text{ch}}$  is specially designed as in (eq.5). The multiplier voltage  $V_M$  is therefore expressed in terms of  $t_1$  in (eq.6).

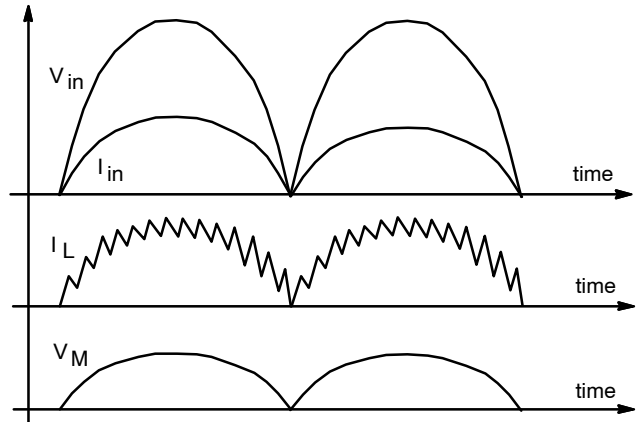
$$I_{\text{ch}} = \frac{C_{\text{ramp}} V_{\text{ref}}}{T} \quad (\text{eq.5})$$

$$V_M = V_{\text{ref}} - \frac{t_1}{C_{\text{ramp}}} \frac{C_{\text{ramp}} V_{\text{ref}}}{T} = V_{\text{ref}} \frac{T - t_1}{T} \quad (\text{eq.6})$$

From (eq.3) and (eq.6), the input impedance  $Z_{\text{in}}$  is re-formulated in (eq.7).

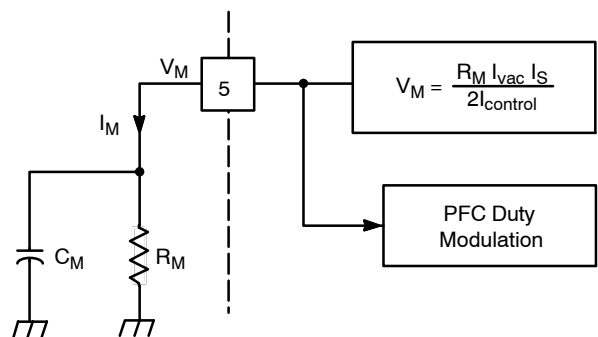
$$Z_{\text{in}} = \frac{V_M V_{\text{out}}}{V_{\text{ref}} I_{L-50}} \quad (\text{eq.7})$$

Because  $V_{\text{ref}}$  and  $V_{\text{out}}$  are roughly constant versus time, the multiplier voltage  $V_M$  is designed to be proportional to the  $I_{L-50}$  in order to have a constant  $Z_{\text{in}}$  for PFC purpose. It is illustrated in Figure 28.



**Figure 28. Multiplier Voltage Timing Diagram**

It can be seen in the timing diagram in Figure 27 that  $V_M$  originally consists of a switching frequency ripple coming from the inductor current  $I_L$ . The duty ratio can be inaccurately generated due to this ripple. This modulation is the so-called “peak current-mode”. Hence, an external capacitor  $C_M$  connected to the multiplier voltage  $V_M$  pin (Pin 5) is essential to bypass the high-frequency component of  $V_M$ . The modulation becomes the so-called “average current-mode” with a better accuracy for PFC.



**Figure 29. External Connection on the Multiplier Voltage Pin**

The multiplier voltage  $V_M$  is generated according to (eq.8).

$$V_M = \frac{R_M I_{\text{vac}} I_s}{2 I_{\text{control}}} \quad (\text{eq.8})$$

Input-voltage current  $I_{\text{vac}}$  is proportional to the RMS input voltage  $V_{\text{ac}}$  as described in (eq.9). The suffix ac

stands for the RMS.  $I_{vac}$  is a constant in the 50 or 60 Hz bandwidth. Multiplier resistor  $R_M$  is the external resistor connected to the multiplier voltage  $V_M$  pin (Pin 5). It is also constant.  $R_M$  directly limits the maximum input power capability and hence its value affects the NCP1653 to operate in either “follower boost mode” or “constant output voltage mode”.

$$I_{vac} = \frac{\sqrt{2} V_{ac} - 4 V}{(R_{vac} + 12 k\Omega)} \approx \frac{V_{ac}}{R'_{vac}} \quad (\text{eq.9})$$

Sense current  $I_S$  is proportional to the inductor current  $I_L$  as described in (eq.10).  $I_L$  consists of the high-frequency component (which depends on di/dt or inductor L) and low-frequency component (which is  $I_{L-50}$ ).

$$I_S = \frac{RCS}{R_S} I_L \quad (\text{eq.10})$$

Control current  $I_{control}$  is a roughly constant current that comes from the PFC output voltage  $V_{out}$  that is a slowly varying signal. The bandwidth of  $I_{control}$  can be additionally limited by inserting an external capacitor  $C_{control}$  to the control voltage  $V_{control}$  pin (Pin 2) in Figure 30. It is recommended to limit  $f_{control}$ , that is the bandwidth of  $V_{control}$  (or  $I_{control}$ ), below 20 Hz typically to achieve power factor correction purpose. Typical value of  $C_{control}$  is between 0.1  $\mu$ F and 0.33  $\mu$ F.

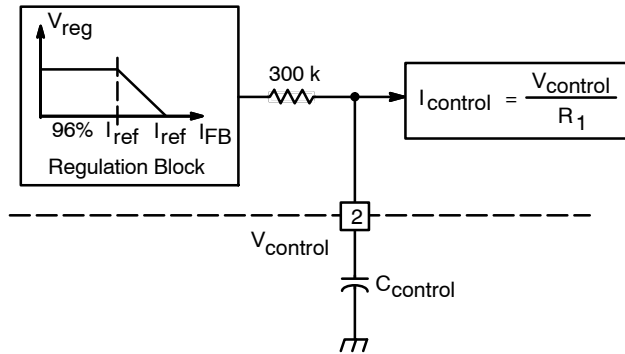


Figure 30.  $V_{control}$  Low-Pass Filtering

$$C_{control} > \frac{1}{2 \pi 300 k\Omega f_{control}} \quad (\text{eq.11})$$

From (eq.7)–(eq.10), the input impedance  $Z_{in}$  is re-formulated in (eq.12).

$$Z_{in} = \frac{R_M R_C S V_{ac} V_{out} I_L}{2 R_S R'_{vac} I_{control} V_{ref} I_{L-50}}$$

$$Z_{in} = \frac{R_M R_C S V_{ac} V_{out}}{2 R_S R'_{vac} I_{control} V_{ref}} \text{ when } I_L = I_{L-50} \quad (\text{eq.12})$$

The multiplier capacitor  $C_M$  is the one to filter the high-frequency component of the multiplier voltage  $V_M$ . The high-frequency component is basically coming from the inductor current  $I_L$ . On the other hand, the filter capacitor  $C_{filter}$  similarly removes the high-frequency component of inductor current  $I_L$ . If the capacitors  $C_M$  and  $C_{filter}$  match with each other in terms of filtering capability,  $I_L$  becomes  $I_{L-50}$ . Input impedance  $Z_{in}$  is roughly constant

over the bandwidth of 50 or 60 Hz and power factor is corrected.

Practically, the differential-mode inductance in the front-ended EMI filter improves the filtering performance of capacitor  $C_{filter}$ . Therefore, the multiplier capacitor  $C_M$  is generally with a larger value comparing to the filter capacitor  $C_{filter}$ .

Input and output power ( $P_{in}$  and  $P_{out}$ ) are derived in (eq.13) when the circuit efficiency  $\eta$  is obtained or assumed. The variable  $V_{ac}$  stands for the RMS input voltage.

$$P_{in} = \frac{V_{ac}^2}{Z_{in}} = \frac{2 R_S R'_{vac} I_{control} V_{ref} V_{ac}}{R_M R_C S V_{out}} \quad (\text{eq.13a})$$

$$\propto \frac{I_{control} V_{ac}}{V_{out}}$$

$$P_{out} = \eta P_{in} = \eta \frac{2 R_S R'_{vac} I_{control} V_{ref} V_{ac}}{R_M R_C S V_{out}} \quad (\text{eq.13b})$$

$$\propto \frac{I_{control} V_{ac}}{V_{out}}$$

### Follower Boost

The NCP1653 operates in follower boost mode when  $I_{control}$  is constant. If  $I_{control}$  is constant based on (eq.13), for a constant load or power demand the output voltage  $V_{out}$  of the converter is proportional to the RMS input voltage  $V_{ac}$ . It means the output voltage  $V_{out}$  becomes lower when the RMS input voltage  $V_{ac}$  becomes lower. On the other hand, the output voltage  $V_{out}$  becomes lower when the load or power demand becomes higher. It is illustrated in Figure 31.

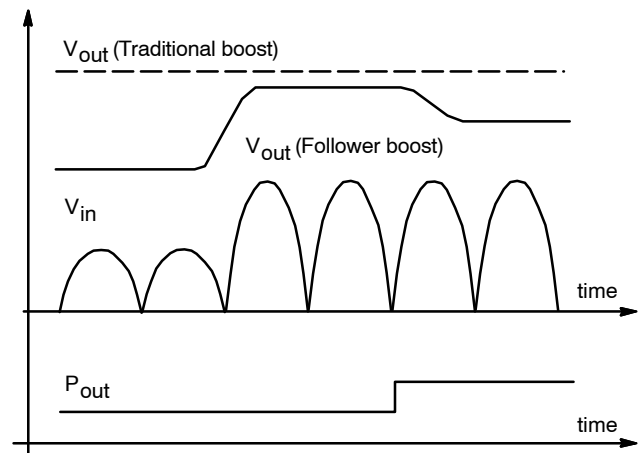


Figure 31. Follower Boost Characteristics

### Follower Boost Benefits

The follower boost circuit offers an opportunity to reduce the output voltage  $V_{out}$  whenever the RMS input voltage  $V_{ac}$  is lower or the power demand  $P_{out}$  is higher. Because of the step-up characteristics of boost converter, the output voltage  $V_{out}$  will always be higher than the input voltage  $V_{in}$  even though  $V_{out}$  is reduced in follower boost operation.

As a result, the on time  $t_1$  is reduced. Reduction of on time makes the loss of the inductor and power MOSFET smaller. Hence, it allows cheaper cost in the inductor and power MOSFET or allows the circuit components to operate at a lower stress condition in most of the time.

**Output Feedback**

The output voltage  $V_{out}$  of the PFC circuit is sensed as a feedback current  $I_{FB}$  flowing into the FB pin (Pin 1) of the device. Since the FB pin voltage  $V_{FB1}$  is much smaller than  $V_{out}$ , it is usually neglected.

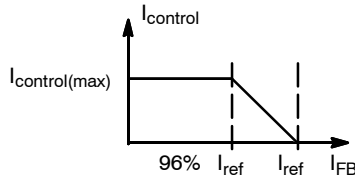
$$I_{FB} = \frac{V_{out} - V_{FB1}}{R_{FB}} \approx \frac{V_{out}}{R_{FB}} \quad (\text{eq.14})$$

where  $R_{FB}$  is the feedback resistor across the FB pin (Pin 1) and the output voltage referring to Figure 2.

Then, the feedback current  $I_{FB}$  represents the output voltage  $V_{out}$  and will be used in the output voltage regulation, undervoltage protection (UVP), and overvoltage protection (OVP).

**Output Voltage Regulation**

Feedback current  $I_{FB}$  which represents the output voltage  $V_{out}$  is processed in a function with a reference current ( $I_{ref} = 200 \mu A$  typical) as shown in regulation block function in Figure 32. The output of the voltage regulation block, low-pass filter on  $V_{control}$  pin and the  $I_{control} = V_{control} / R_1$  block is in Figure 30 is control current  $I_{control}$ . And the input is feedback current  $I_{FB}$ . It means that  $I_{control}$  is the output of  $I_{FB}$  and it can be described as in Figure 32. There are three linear regions including: (1)  $I_{FB} < 96\% \times I_{ref}$ , (2)  $96\% \times I_{ref} < I_{FB} < I_{ref}$ , and (3)  $I_{FB} > I_{ref}$ . They are discussed separately as follows:



**Figure 32. Regulation Block**

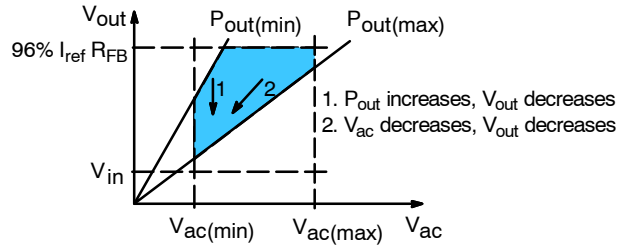
**Region (1):  $I_{FB} < 96\% \times I_{ref}$**

When  $I_{FB}$  is less than 96% of  $I_{ref}$  (i.e.,  $V_{out} < 96\% R_{FB} \times I_{ref}$ ), the NCP1653 operates in follower boost mode. The regulation block output  $V_{reg}$  is at its maximum value.  $I_{control}$  becomes its maximum value (i.e.,  $I_{control} = I_{control(max)} = I_{ref}/2 = 100 \mu A$ ) which is a constant. (eq.13) becomes (eq.15).

$$V_{out} = \eta \frac{2 RS R'_{vac} I_{control(max)} V_{ref} V_{ac}}{RM RCS P_{out}} \propto \frac{V_{ac}}{P_{out}} \quad (\text{eq.15})$$

The output voltage  $V_{out}$  is regulated at a particular level with a particular value of RMS input voltage  $V_{ac}$  and output power  $P_{out}$ . However, this output level is not constant and

depending on different values of  $V_{ac}$  and  $P_{out}$ . The follower boost operating area is illustrated in Figure 33.



**Figure 33. Follower Boost Region**

**Region (2):  $96\% \times I_{ref} < I_{FB} < I_{ref}$**

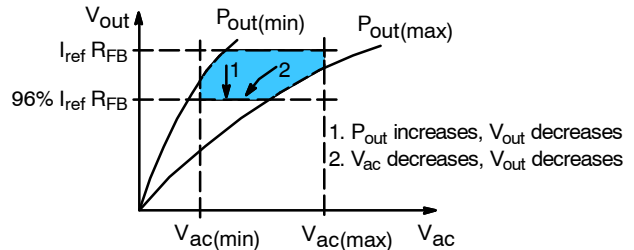
When  $I_{FB}$  is between 96% and 100% of  $I_{ref}$  (i.e.,  $96\% R_{FB} \times I_{ref} < V_{out} < R_{FB} \times I_{ref}$ ), the NCP1653 operates in constant output voltage mode which is similar to the follower boost mode characteristic but with narrow output voltage range. The regulation block output  $V_{reg}$  decreases linearly with  $I_{FB}$  in the range from 96% of  $I_{ref}$  to  $I_{ref}$ . It gives a linear function of  $I_{control}$  in (eq.16).

$$I_{control} = \frac{I_{control(max)}}{0.04} \left( 1 - \frac{V_{out}}{R_{FB} I_{ref}} \right) \quad (\text{eq.16})$$

Resolving (eq.16) and (eq.13),

$$V_{out} = \frac{V_{ac}}{\left( \frac{RM RCS}{2 RS R'_{vac} V_{ref}} \frac{0.04}{I_{control(max)}} \frac{P_{out}}{\eta} + \frac{V_{ac}}{R_{FB} I_{ref}} \right)} \quad (\text{eq.17})$$

According to (eq.17), output voltage  $V_{out}$  becomes  $R_{FB} \times I_{ref}$  when power is low ( $P_{out} \approx 0$ ). It is the maximum value of  $V_{out}$  in this operating region. Hence, it can be concluded that output voltage increases when power decreases. It is similar to the follower boost characteristic in (eq.15). On the other hand in (eq.17), output voltage  $V_{out}$  becomes  $R_{FB} \times I_{ref}$  when RMS input voltage  $V_{ac}$  is very high. It is the maximum value of  $V_{out}$  in this operating region. Hence, it can also be concluded that output voltage increases when RMS input voltage increases. It is similar to another follower boost characteristic in (eq.15). This characteristic is illustrated in Figure 34.



**Figure 34. Constant Output Voltage Region**

**Region (3):  $I_{FB} > I_{ref}$**

When  $I_{FB}$  is greater than  $I_{ref}$  (i.e.,  $V_{out} > R_{FB} \times I_{ref}$ ), the NCP1653 provides no output or zero duty ratio. The regulation block output  $V_{reg}$  becomes 0 V.  $I_{control}$  also becomes zero. The multiplier voltage  $V_M$  in (eq.8)

becomes its maximum value and generates zero on time  $t_1$ . Then,  $V_{out}$  decreases and the minimum can be  $V_{out} = V_{in}$  in a boost converter. Going down to  $V_{in}$ ,  $V_{out}$  automatically enters the previous two regions (i.e., follower boost region or constant output voltage region) and hence output voltage  $V_{out}$  cannot reach input voltage  $V_{in}$  as long as the NCP1653 provides a duty ratio for the operation of the boost converter.

In conclusion, the NCP1653 circuit operates in one of the following conditions:

**Constant output voltage mode:** The output voltage is regulated around the range between 96% and 100% of  $R_{FB} \times I_{ref}$ . The output voltage is described in (eq.16). Its behavior is similar to a follower boost.

**Follower boost mode:** The output voltage is regulated under 96% of  $R_{FB} \times I_{ref}$  and  $I_{control} = I_{control(max)} = I_{ref}/2 = 100 \mu A$ . The output voltage is described in (eq.15).

### Overvoltage Protection (OVP)

When the feedback current  $I_{FB}$  is higher than 107% of the reference current  $I_{ref}$  (i.e.,  $V_{out} > 107\% R_{FB} \times I_{ref}$ ), the Drive Output (Pin 7) of the device goes low for protection. The circuit automatically resumes operation when the feedback current becomes lower than 107% of the reference current  $I_{ref}$ .

The maximum OVP threshold is limited to  $230 \mu A$  which corresponds to  $230 \mu A \times 1.92 M\Omega + 2.5 V = 444.1 V$  when  $R_{FB} = 1.92 M\Omega$  ( $680 k\Omega + 680 k\Omega + 560 k\Omega$ ) and  $V_{FB1} = 2.5 V$  (for the worst case referring to Figure 11). Hence, it is generally recommended to use 450 V rating output capacitor to allow some design margin.

### Undervoltage Protection (UVP)

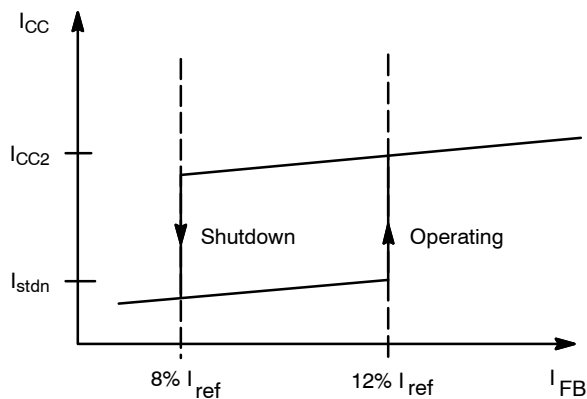


Figure 35. Undervoltage Protection

When the feedback current  $I_{FB}$  is less than 8% of the reference current  $I_{ref}$  (i.e., the output voltage  $V_{out}$  is less than 8% of its nominal value), the device is shut down and consumes less than  $50 \mu A$ . The device automatically starts operation when the output voltage goes above 12% of the nominal regulation level. In normal situation of boost converter configuration, the output voltage  $V_{out}$  is always greater than the input voltage  $V_{in}$  and the feedback current  $I_{FB}$  is always greater than 8% and 12% of the nominal level

to enable the NCP1653 to operate. Hence, UVP happens when the output voltage is abnormally undervoltage, the FB pin (Pin 1) is opened, or the FB pin (Pin 1) is manually pulled low.

### Soft-Start

The device provides no output (or no duty ratio) when the  $V_{control}$  (Pin 2) voltage is zero (i.e.,  $V_{control} = 0 V$ ). An external capacitor  $C_{control}$  connected to the  $V_{control}$  pin provides a gradually increment of the  $V_{control}$  voltage (or the duty ratio) in the startup and hence provides a soft-start feature.

### Current Sense

The device senses the inductor current  $I_L$  by the current sense scheme in Figure 36. The device maintains the voltage at the CS pin (Pin 4) to be zero voltage (i.e.,  $V_S \approx 0 V$ ) so that (eq.10) can be formulated.

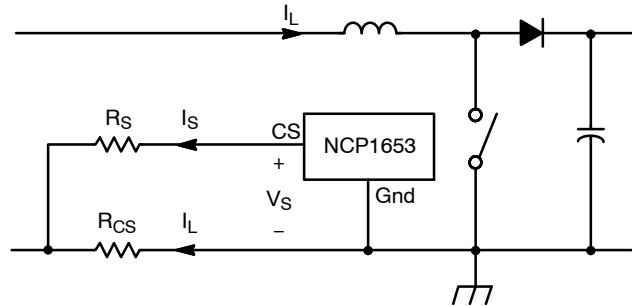


Figure 36. Current Sensing

This scheme has the advantage of the minimum number of components for current sensing and the inrush current limitation by the resistor  $R_{CS}$ . Hence, the sense current  $I_S$  represents the inductor current  $I_L$  and will be used in the PFC duty modulation to generate the multiplier voltage  $V_M$ , Overpower Limitation (OPL), and overcurrent protection.

### Overcurrent Protection (OCP)

Overcurrent protection is reached when  $I_S$  is larger than  $I_{S(OCP)}$  ( $200 \mu A$  typical). The offset voltage of the CS pin is typical 10 mV and it is neglected in the calculation. Hence, the maximum OCP inductor current threshold  $I_{L(OCP)}$  is obtained in (eq.15).

$$I_{L(OCP)} = \frac{R_S I_{S(OCP)}}{R_{CS}} = \frac{R_S}{R_{CS}} \times 200 \mu A \quad (\text{eq.18})$$

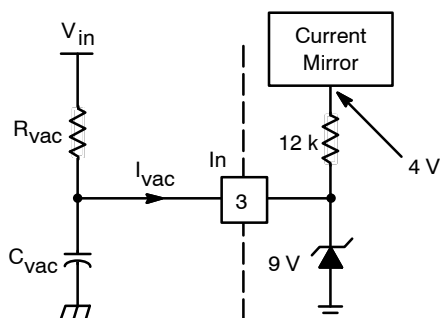
When overcurrent protection threshold is reached, the Drive Output (Pin 7) of the device goes low. The device automatically resumes operation when the inductor current goes below the threshold.

### Input Voltage Sense

The device senses the RMS input voltage  $V_{ac}$  by the sensing scheme in Figure 37. The internal current mirror is with a typical 4 V offset voltage at its input so that the current  $I_{vac}$  can be derived in (eq.9). An external capacitor  $C_{vac}$  is to maintain the In pin (Pin 3) voltage in the



calculation to always be the peak of the sinusoidal voltage due to very little current consumption (i.e.,  $V_{in} = \sqrt{2} V_{ac}$  and  $I_{vac} \approx 0$ ). This  $I_{vac}$  current represents the RMS input voltage  $V_{ac}$  and will be used in overpower limitation (OPL) and the PFC duty modulation.



**Figure 37. Input Voltage Sensing**

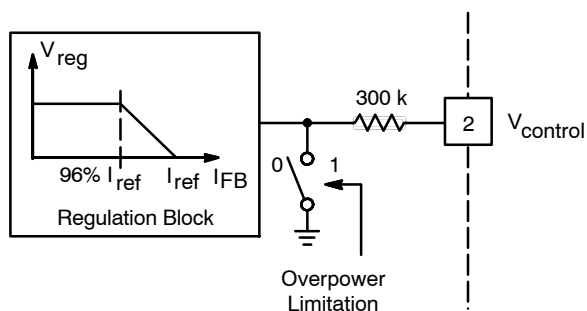
There is an internal 9 V ESD Zener Diode on the pin. Hence, the value of  $R_{vac}$  is recommended to be at least 938 kΩ for possibly up to 400 V instantaneous input voltage.

$$\frac{R_{vac}}{400\text{ V} - 9\text{ V}} > \frac{12\text{ k}\Omega}{9\text{ V} - 4\text{ V}}$$

$$R_{vac} > 938\text{ k}\Omega \quad (\text{eq.19})$$

**Overpower Limitation (OPL)**

Sense current  $I_S$  represents the inductor current  $I_L$  and hence represents the input current approximately. Input-voltage current  $I_{vac}$  represents the RMS input voltage  $V_{ac}$  and hence represents the input voltage. Their product ( $I_S \times I_{vac}$ ) represents an approximated input power ( $I_L \times V_{ac}$ ).



**Figure 38. Overpower Limitation Reduces  $V_{control}$**

When the product ( $I_S \times I_{vac}$ ) is greater than a permissible level  $3\text{ nA}^2$ , the output  $V_{reg}$  of the regulation block is pulled to 0 V. It makes  $V_{control}$  to be 0 V indirectly and  $V_M$  is pulled to be its maximum. It generates the minimum duty ratio or no duty ratio eventually so that the input power is

limited. The OPL is automatically deactivated when the product ( $I_S \times I_{vac}$ ) becomes lower than the  $3\text{ nA}^2$  level. This  $3\text{ nA}^2$  level corresponds to the approximated input power ( $I_L \times V_{ac}$ ) to be smaller than the particular expression in (eq.20).

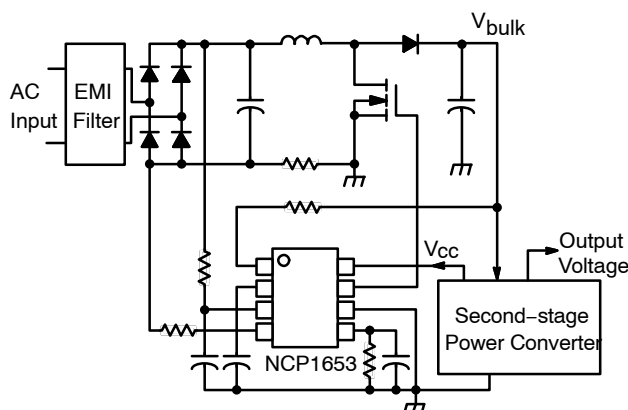
$$I_S I_{vac} < 3\text{ nA}^2$$

$$\left( I_L \cdot \frac{R_{CS}}{R_S} \right) \times \left( V_{ac} \cdot \frac{\sqrt{2}}{R_{vac} + 12\text{ k}\Omega} \right) < 3\text{ nA}^2$$

$$I_L \cdot V_{ac} < \frac{R_S}{R_{CS}} \frac{R_{vac} + 12\text{ k}\Omega}{\sqrt{2}} 3\text{ nA}^2 \quad (\text{eq.20})$$

**Biasing the Controller**

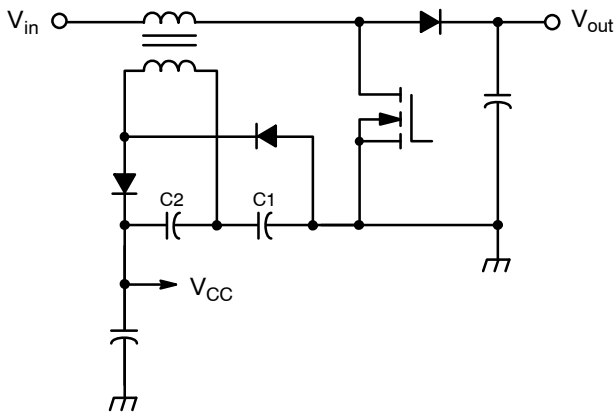
It is recommended to add a typical 1 nF to 100 nF decoupling capacitor next to the  $V_{CC}$  pin for proper operation. When the NCP1653 operates in follower boost mode, the PFC output voltage is not always regulated at a particular level under all application range of input voltage and load power. It is not recommended to make a low-voltage bias supply voltage by adding an auxiliary winding on the PFC boost inductor. Alternatively, it is recommended to get the  $V_{CC}$  biasing supply from the second-stage power conversion stage as shown in Figure 39.



**Figure 39. Recommended Biasing Scheme in Follower Boost Mode**

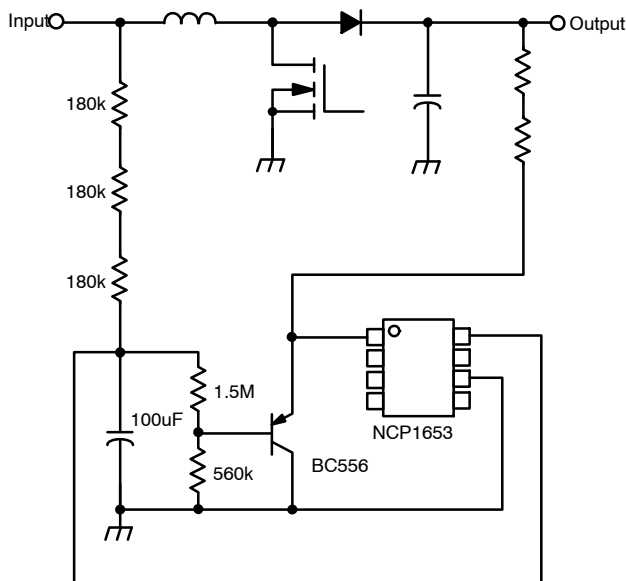
When the NCP1653 operates in constant output voltage mode, it is possible to make a low-voltage bias supply by adding an auxiliary winding on the PFC boost inductor in Figure 40. In PFC boost circuit, the input is the rectified AC voltage and it is non-constant versus time that makes the auxiliary winding voltage also non-constant. Hence, the configuration in Figure 40 charges the voltages in capacitors  $C1$  and  $C2$  to  $n \times (V_{out} - V_{in})$  and  $n \times V_{in}$  and  $n$  is the turn ratio. As a result, the stack of the voltages is  $n \times V_{out}$  that is constant and can be used as a biasing voltage.

## NCP1653, NCP1653A



**Figure 40. Self-biasing Scheme in Constant Output Voltage Mode**

When the NCP1653 circuit is required to be startup independently from the second-stage converter, it is recommended to use a circuit in Figure 41. When there is no feedback current ( $I_{FB} = 0 \mu\text{A}$ ) applied to FB pin (Pin 1), the NCP1653  $V_{CC}$  startup current is as low ( $50 \mu\text{A}$  maximum). It is good for saving the current to charge the  $V_{CC}$  capacitor. However, when there is some feedback current the startup current rises to as high as  $1.5 \text{ mA}$  in the  $V_{CC} < 4 \text{ V}$  region. That is why the circuit of Figure 41 can be implemented: a PNP bipolar transistor derives the feedback current to ground at low  $V_{CC}$  levels ( $V_{CC} < 4 \text{ V}$ ) so that the startup current keeps low and an initial voltage can be quickly built up in the  $V_{CC}$  capacitor. The values in Figure 41 are just for reference.



**Figure 41. Recommended Startup Biasing Scheme**

### $V_{CC}$ Undervoltage Lockout (UVLO)

The device typically starts to operate when the supply voltage  $V_{CC}$  exceeds  $13.25 \text{ V}$ . It turns off when the supply voltage  $V_{CC}$  goes below  $8.7 \text{ V}$ . An  $18 \text{ V}$  internal ESD Zener Diode is connected to the  $V_{CC}$  pin (Pin 8) to prevent excessive supply voltage. After startup, the operating range is between  $8.7 \text{ V}$  and  $18 \text{ V}$ .

### Thermal Shutdown

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds  $150^\circ\text{C}$ . The output stage is then enabled once the temperature drops below typically  $120^\circ\text{C}$  (i.e.,  $30^\circ\text{C}$  hysteresis). The thermal shutdown is provided to prevent possible device failures that could result from an accidental overheating.

### Output Drive

The output stage of the device is designed for direct drive of power MOSFET. It is capable of up to  $\pm 1.5 \text{ A}$  peak drive current and has a typical rise and fall time of  $88$  and  $61.5 \text{ ns}$  with a  $2.2 \text{ nF}$  load.



# NCP1653, NCP1653A

## Application Schematic

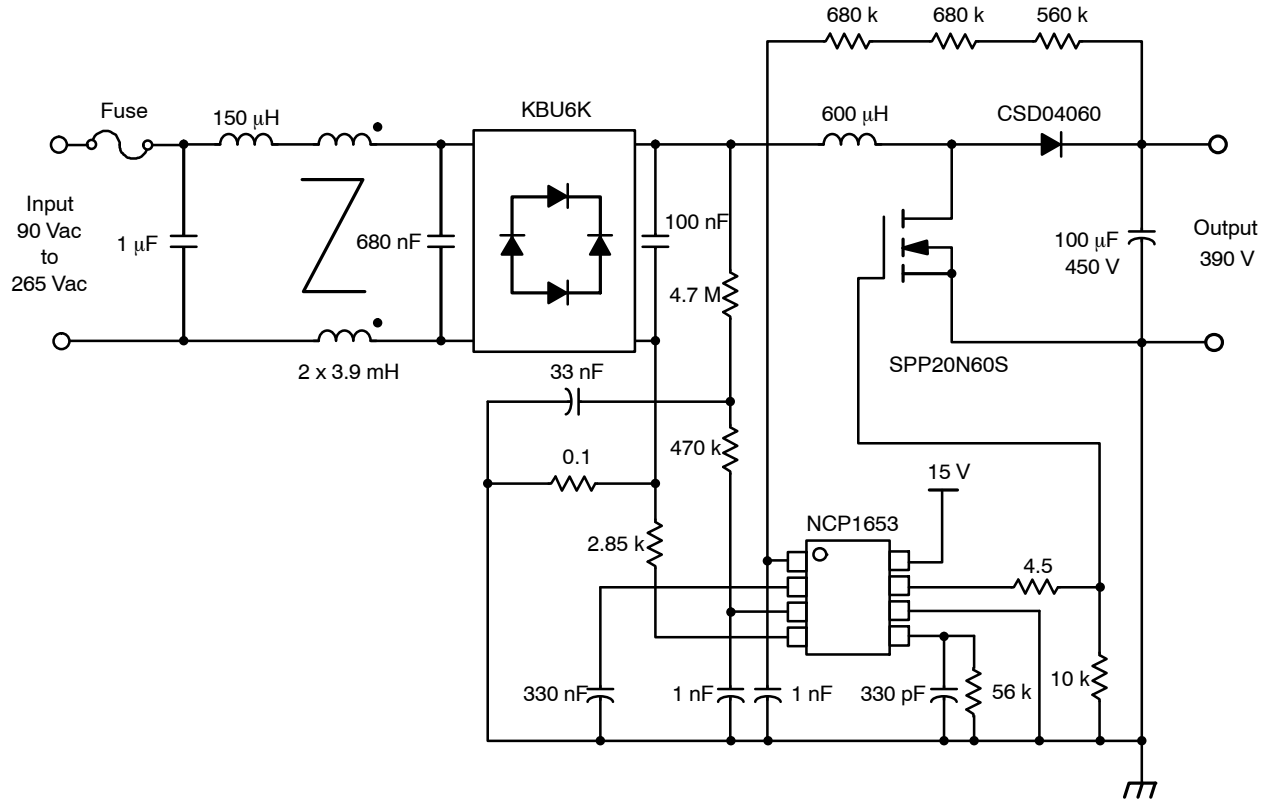


Figure 42. 300 W 100 kHz Power Factor Correction Circuit

Table 1. Total Harmonic Distortion and Efficiency

Input Voltage (V)	Input Power (W)	Output Voltage (V)	Output Current (A)	Power Factor	Total Harmonic Distortion (%)	Efficiency (%)
110	331.3	370.0	0.83	0.998	4	93
110	296.7	373.4	0.74	0.998	4	93
110	157.3	381.8	0.38	0.995	7	92
110	109.8	383.5	0.26	0.993	9	91
110	80.7	384.4	0.19	0.990	10	91
110	67.4	385.0	0.16	0.988	10	91
220	311.4	385.4	0.77	0.989	9	95
220	215.7	386.2	0.53	0.985	8	95
220	157.3	386.4	0.38	0.978	9	93
220	110.0	386.7	0.27	0.960	11	95
220	80.2	386.5	0.19	0.933	14	92
220	66.9	386.6	0.16	0.920	15	92

# NCP1653, NCP1653A

## APPENDIX I – SUMMARY OF EQUATIONS IN NCP1653 BOOST PFC

Description	Follower Boost Mode	Constant Output Voltage Mode
Boost Converter	$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2} = \frac{T}{T - t_1}$ $\rightarrow \frac{V_{out} - V_{in}}{V_{out}} = \frac{t_1}{t_1 + t_2} = \frac{t_1}{T}$	Same as Follower Boost Mode
Input Current Averaged by Filter Capacitor	$I_{in} = I_L - 50$	Same as Follower Boost Mode
Nominal Output Voltage ( $I_{FB} = 200 \mu A$ )	$V_{out(nom)} = I_{FB}R_{FB} + V_{FB1}$ $\approx I_{FB}R_{FB} = 200 \mu A \cdot R_{FB}$	Same as Follower Boost Mode
Feedback Pin Voltage $V_{FB1}$	Please refer to Figure 11.	Same as Follower Boost Mode
Output Voltage	$V_{in} < V_{out} < 192 \mu A \cdot R_{FB}$	$192 \mu A \cdot R_{FB} < V_{out} < 200 \mu A \cdot R_{FB}$
Inductor Current Peak-Peak Ripple	$\Delta I_L(pk - pk) < 2 \cdot I_L - 50$	Same as Follower Boost Mode
Control Current	$I_{control} = I_{control(max)} = \frac{I_{ref}}{2} = 100 \mu A$	$I_{control} = \frac{I_{control(max)}}{0.04} \left( 1 - \frac{V_{out}}{R_{FB}I_{ref}} \right)$ and $I_{control} < I_{control(max)} = 100 \mu A$
Switching Frequency	$f = 67$ or $100$ kHz	Same as Follower Boost Mode
Minimum Inductor for CCM	$L > L_{(CRM)} = \frac{V_{out} - V_{in}}{V_{out}} \frac{V_{in}}{\Delta I_L(pk - pk)} \frac{1}{f}$	Same as Follower Boost Mode
Input Impedance	$Z_{in} = \frac{R_M R_{CS} V_{ac} V_{out}}{R_S R'_{vac} I_{ref} V_{ref}}$	$Z_{in} = \frac{R_M R_{CS} V_{ac} V_{out}}{2 R_S R'_{vac} I_{control} V_{ref}}$
Input Power	$P_{in} = \frac{R_S R'_{vac} I_{ref} V_{ref} V_{ac}}{R_M R_{CS} V_{out}}$	$P_{in} = \frac{2 R_S R'_{vac} V_{ref} I_{control} V_{ac}}{R_M R_{CS} V_{out}}$
Output Power	$P_{out} = \eta P_{in} = \frac{\eta R_S R'_{vac} I_{ref} V_{ref} V_{ac}}{R_M R_{CS} V_{out}}$	$P_{out} = \frac{\eta^2 R_S R'_{vac} V_{ref} I_{control} V_{ac}}{R_M R_{CS} V_{out}}$
Maximum Input Power when $I_{control} = 100 \mu A$	$P_{in(max)} = P_{in} = \frac{R_S R'_{vac} I_{ref} V_{ref} V_{ac}}{R_M R_{CS} V_{out}}$	Circuit will enter follower boost region when maximum power is reached.
Current Limit	$I_L(OCP) = \frac{R_S}{R_{CS}} \cdot 200 \mu A$	Same as Follower Boost Mode
Power Limit	$I_L \cdot V_{AC} < \frac{R_S}{R_{CS}} \frac{R_{vac} + 12 k\Omega}{\sqrt{2}} \cdot 3 nA^2$	Same as Follower Boost Mode
Output Overvoltage	$V_{out(OVP)} = 107\% \cdot V_{out(nom)}$ $\approx 214 \mu A \cdot R_{FB}$	Same as Follower Boost Mode
Output Undervoltage	$V_{out(UVP - on)} = 8\% \cdot V_{out(nom)}$ $\approx 16 \mu A \cdot R_{FB}$ $V_{out(UVP - off)} = 12\% \cdot V_{out(nom)}$ $\approx 24 \mu A \cdot R_{FB}$	Same as Follower Boost Mode
Input Voltage Sense Pin Resistor $R_{vac}$	$R_{vac} > 938 k\Omega$ and $R'_{vac} = \frac{R_{vac} + 12 k\Omega}{\sqrt{2}}$	Same as Follower Boost Mode
PWM Comparator Reference Voltage	$V_{ref} = 2.62 V$	Same as Follower Boost Mode

## NCP1653, NCP1653A

### ORDERING INFORMATION

Device	Package	Shipping†	Switching Frequency
NCP1653PG	PDIP-8 (Pb-Free)	50 Units / Rail	100 kHz
NCP1653DR2G	SO-8 (Pb-Free)	2500 Units / Tape & Reel	
NCP1653APG	PDIP-8 (Pb-Free)	50 Units / Rail	67 kHz
NCP1653ADR2G	SO-8 (Pb-Free)	2500 Units / Tape & Reel	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

**PDIP-8**  
CASE 626-05  
ISSUE P

DATE 22 APR 2015



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

**GENERIC MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- STYLE 1:  
 PIN 1. AC IN  
 2. DC + IN  
 3. DC - IN  
 4. AC IN  
 5. GROUND  
 6. OUTPUT  
 7. AUXILIARY  
 8. V<sub>CC</sub>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*

### SOLDERING FOOTPRINT\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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